SA1000
Fixed Disk Drive

Service Manual

Shugart

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Section 1

Theory of Operations

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1.0 INTRODUCTION

1.1 GENERAL DESCRIPTION

The Shugart Model 1000 series disk drive is a random access storage device with one or two non-removable 8" disks as storage media. Each disk surface employs one movable head to service 256 data tracks. The two models of the SA1000 series are the SA1002 and the SA1004 with single and double platters respectively. The SA1002 provides 5 megabytes accessed by 2 movable heads and the SA1004 provides 10 megabytes accessed by 4 movable heads.

Low cost and unit reliability are achieved through the use of a unique band actuator design. The inherent simplicity of mechanical construction and electronic controls allows maintenance free operation throughout the life of the drive.

Mechanical and contamination protection for the head, actuator and disks are provided by an impact resistant plastic and die cast aluminum enclosure. A self contained recirculating system supplies clean air through a 0.3 micron absolute filter. Another 0.3 micron absolute filter allows pressure equalization with ambient air without chance of contamination.

The SA1000 fixed disk drive's interface is similar to the Shugart 8" family of floppy disk drives. The SA1000 is designed to fit into the same physical space as the 8" floppies. However, existing floppy controllers are not compatible with the SA1000 due to differences in the data transfer rates.

Key Features:

- Storage Capacity of 5.33 or 10.67 megabytes.
- Winchester design reliability.
- Same physical size and identical mounting configuration as the SA800/850 floppies.
- Uses the same D.C. voltages as the SA800/850 floppies.
- Proprietary Fas Flex III band actuator.
- 4.34 Mbits/second transfer rate.
- Simple floppy-like interface.

1.2 WINCHESTER TECHNOLOGY

The SA1000 disk drive employs Winchester technology. The term Winchester refers to several unique features about the drive. They are:

* Environmentally sealed chamber for heads and disks.

* Disk surface lubricated to facilitate magnetic head take off and landing without damage to the media (The heads can land randomly anywhere on the surface of the media).

* A head that flies 19 micro inches above the surface of the media.

* Reduced head load force of 9.5 grams which allows the heads to rest on the surface of media prior to take off (The spindle speed for head take off is approximately 500 rpm).

The close proximity of the heads to the recording media permits recording densities of 6270 bits-per-inch. This recording density allows 10 megabytes of data to be stored on an 8-inch drive. Sealing the chamber that houses the disk and head assemblies prevents contaminants from reaching the disk surface. The 0.3 micron absolute breather and recirculating filters keep the environment inside the chamber free from undesirable particulate contaminants.

UNDER NO CONDITION MUST THE DRIVE BE UNSEALED IN THE FIELD. A CLASS 100 CLEAN ROOM ENVIRONMENT IS NEEDED FOR UNDER-THE-BUBBLE REPAIR.

1.3 SPECIFICATION SUMMARY

1.3.1 PHYSICAL SPECIFICATIONS

Environmental Limits

Ambient Temperature =	50° to 115°F (10° to 46°C)
Relative Humidity =	8% to 80%
Maximum Wet Bulb =	78°F non-condensing

AC Power Requirements

50/60 Hz ± 0.5Hz

100/115 VAC Installations =	90-127V at 0.75A typical
200/230 VAC Installations =	180-253V at 0.38A typical

DC Voltage Requirements

+24VDC ± 10% 2.8A typical during stepping
(0.2A typical steady state, non stepping)
+5VDC ± 2.0A typical during stepping
(3.6A typical non-stepping)
-5VDC ± 5% (-7 to -16VDC optional) .2A typical

Mechanical Dimensions

	Rack Mount	**Standard Mount**
Height =	4.62 in. (117.3mm)	4.62 in. (117.3mm)
Width =	8.55 in (217.2mm)	9.50 in. (241.3mm)
Depth =	14.25 in. (362.0mm)	14.25 in. (362.0mm)

Heat Dissipation = 511 BTU/Hr. typical (150 Watts)

1.3.2 RELIABILITY SPECIFICATIONS

MTBF: 8,000 POH typical usage

PM: None required

MTTR: 30 minutes
Component Life: 5 years
Error Rates:

Soft Read Errors:	1 per 10^{10} bits read
Hard Read Errors:	1 per 10^{12} bits read
Seek Errors:	1 per 10^{6} seeks

1.3.3 PERFORMANCE SPECIFICATIONS

Capacity	**SA1002**	**SA1004**
Unformatted		
Per Drive	5.33 Mbytes	10.67 Mbytes
Per Surface	2.67 Mbytes	2.67 Mbytes
Per Track	10.4 Kbytes	10.4 Kbytes
Formatted		
Per Drive	4.2 Mbytes	8.4 Mbytes
Per Surface	2.1 Mbytes	2.1 Mbytes
Per Track	8.2 Kbytes	8.2 Kbytes
Per Sector	256 bytes	256 bytes
Sectors/Track	32	32
Transfer Rate	4.34 Mbits/sec	4.34 Mbits/sec

Access Time		
Track to Track	19 msec	19 msec
Average	70 msec	70 msec
Maximum	150 msec	150 msec
Average Latency	9.6 msec	9.6 msec

1.3.4 FUNCTIONAL SPECIFICATIONS

Rotational Speed	3125 rpm	3125 rpm
Recording Density	6270 bpi	6270 bpi
Flux Density	6270 fci	6270 fci
Track Density	172 tpi	172 tpi
Cylinders	256	256
Tracks	512	1024
R/W Heads	2	4
Disks	1	2

2.0 THEORY OF OPERATION

2.1 INTRODUCTION

This section will functionally describe the major circuits of the SA1000. For interface timing, refer to SA1000 OEM manual P/N 39010.

2.2 POWER ON RESET CIRCUIT (POR)

In order to generate a -POR (Power on Reset) signal, a simple switching circuit on the control PCB is used. This circuit utilizes capacitor C4, transistor Q5 and two biasing resistors R67 and R68. When initial D.C. voltages are applied to the drive, C4 charges up from 0 volts preventing Q5 from turning on. This establishes a low at the output of IC 5C. It takes approximately 50ms for C4 to charge up enough to turn on Q5. Once Q5 is turned on, IC 5C8 will remain high until power is removed.

The following latches are cleared during the power-on phase:

- Resets the fault latch, 6D on the Control PCB.
- At the stepper PCB - POR loads counter chip 3F with a hex count of 3, which is translated at the decoder chip 2F to $0A_2$, $0B_1$ (phase A).
- Resets the seek complete latch 2A, allows seek complete to be active at the interface if the read/write heads are located at Track 000.
- Sets the Auto-Recal latch 3C on the stepper PCB.
- Clears the step enable latch, 1C on the stepper PCB.
- Loads track count buffer IC's 5E and 4B to a hex count of FF on the stepper PCB.

After the reset initialization is completed the drive waits for the ready condition to occur.

2.3 DRIVE READY (CONTROL PCB/STEPPER PCB)

The drive ready condition occurs when the disk spindle speed is above 95% of its nominal velocity (@ 2968 RPM's). The ready circuit is derived by comparing the time between two successive index pulses to a fixed time reference. The index detection circuit consists of an op amp differentiator and a one shot schmitt trigger. A zero detection at the output of the differentiator circuit would generate a 10μs pulse at the output of IC 7B7. The frequency of the index pulse is depended upon the rated rotational velocity of the disk. The frequency period is equal to 19.2ms when the disk is rotating at the rated speed (3125 rpm).

At the Stepper PCB an active low index signal presets the parallel inputs to counters 1E and 2E. These counters are clocked by a 271Khz signal. It takes approximately 20 ms for 1E and 2E to overflow. A low, out of counter 1E14, resets speed latches 1D and 5F. The speed latches will remain cleared if the time between two index pulses is greater than 20.04 ms, indicating a not ready condition. When the disk is rotating above 95% of its nominal rotational speed, incoming indexes will preset 1E and 2E before they time out. The next index signal will set latch 5F and 5F6 will go low indicating an active ready condition.

2.4 AUTO RECAL (STEPPER LOGIC P.C.B.)

An Auto Recal is performed if two basic conditions are satisfied: One is that drive ready has to be in the active state, and the other is that the heads must not be positioned over track zero. Assuming that these conditions are met, the following logic functions are performed. The Index signal is gated through IC's 3C and 4F. The Step Enable signal is in the inactive state, which allows the index signal to be used as a pseudo step signal. The Auto Recal latch (3C) is currently in the set position, indicating the direction of motion of the read/write heads will begin to recalibrate in the normal mode of operation until the track zero phase (phase A) is detected. The seek settle timer 1B and 2B will time out in approximately 18ms, activating Seek Complete at the interface. The drive is now ready for normal operation.

2.5 STEPPING

The STEP interface line is a control signal, which causes the read/write heads to move in the direction defined by the DIRECTION IN line. The Direction In line must be stable at least 100ns before the leading edge of the Step pulse.

There are two basic modes of operation of stepping the read/write heads, the normal mode and the buffered mode. In order to implement either of these two modes of operation, there are several conditions that must be initiated before stepping can be accomplished.

1. Write Gate must be inactive.

2. Drive Select must be active.

3. Ready must be active, and Seek Complete true.

2.5.1 BUFFERED MODE STEPPING

In this mode, the step pulses are received at a high rate (pulse period separation between 3.0μs and 200μs), and buffered into step counters 4B and 5E. Once all step pulses have been received, step rate timer 5A14 will output a low, which is gated through IC's 3D10, 3E5 and 4F5. This logic function is used to prevent any more step pulses from being received.

The actual stepping operation will now begin, depending upon the step count loaded into the step count buffers, 4B and 5E. For discussion, assume a 20_{10} track seek operation.

Counters 4B and 5E will hold a count of 3_{16} and 1_{16} respectively. The count of IC 4B will be compared to the count of IC 3A (this count currently equals zero). Since IC 4B's count is greater than the count of IC 3A, IC 4A, Pin 5 will output a logical one. A high signal out of 4A will select the outputs from counters 3A through 3B. This particular count will be used as an address to prom 5B. The firmware control for each address is designed to select the appropriate step rate time (see figure 1). The approximate time for the first step rate is 200μs (Prom address 16_{10}) and the second step rate time is approximately 560μs (Prom address 17_{10}). The output from IC 5A, Pin 14, will clock the divide-by-2 flip flop at 1D. The output (low to high transition) from the flip flop (IC 1D, Pin 9), has several important functions:

— Enables the 14μs window generator circuit (step enable signal).

— Enables sequencing from the phase counter.

The phase counter will either count up or down depending upon the direction line. (For phase counter timing see figure 2).

— Enables the down count from counter 4B.

The step count from counter 4B is continuously compared to the count of 3A, until 3A becomes greater than the count of 4B. At this time data selector 3B will select the lower value step count of IC 4B. Slower and slower step times are selected (ramping down) until the step time is at the rate of the initial step.

For longer seeks, the step speed will increase (ramp up) during the first 15 steps, until the maximum step speed is reached. The speed will be maintained until only 15 steps remain. Now the step speed is decreased (ramp down) gradually down to the initial 1120 usec rate. The purpose of ramping up is to decrease the total seek time, and the purpose of ramping down is to slow the stepper mass down in order that a settle time of 18 msec, can be maintained.

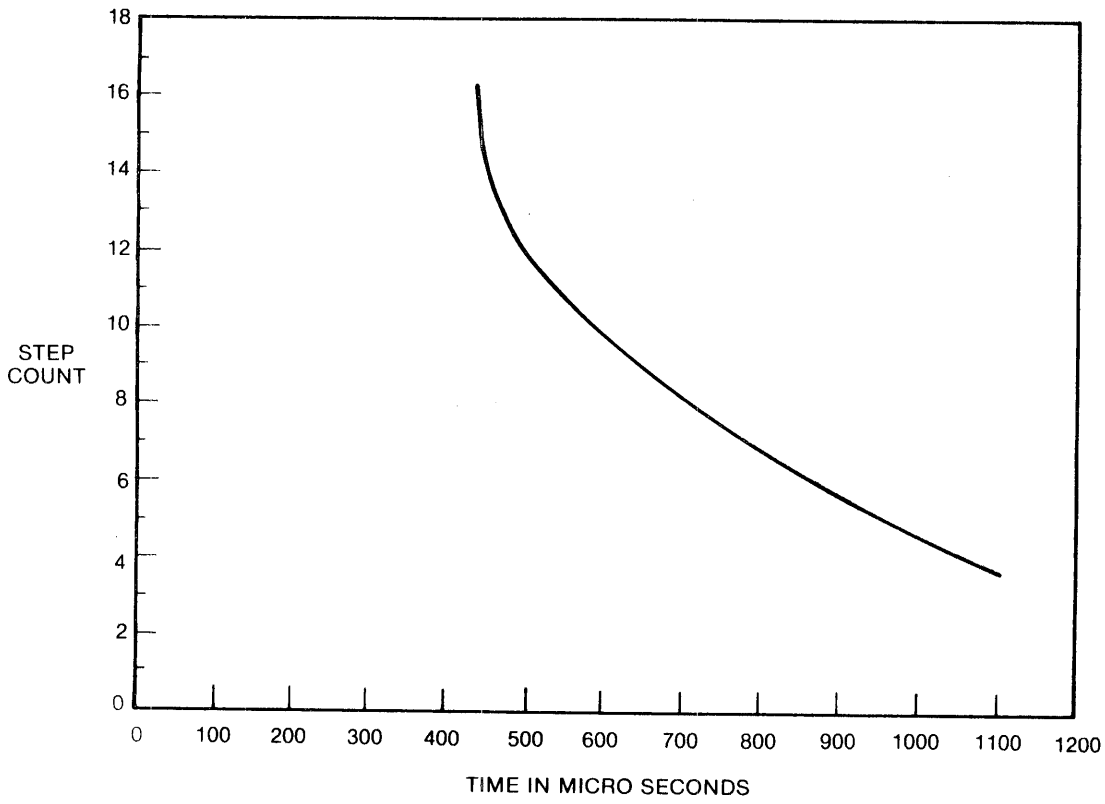
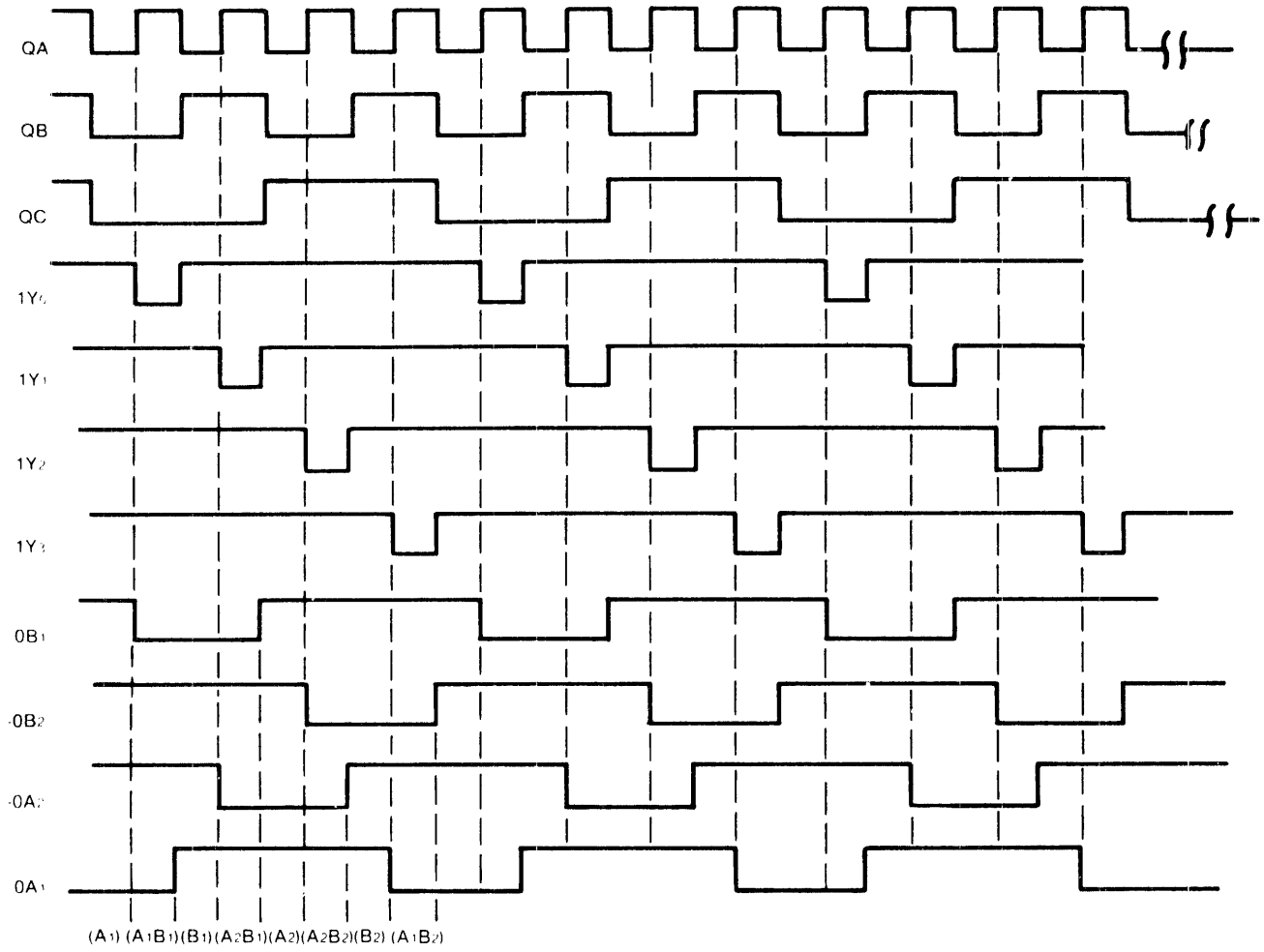


FIGURE 1. TYPICAL STEP RATE RAMP CURVE

GENERAL STEP PHASE TIMING



TRUTH TABLE FOR PHASE SEQUENCES

	QC	QB	QA	0A1	0B1	0A2	0B2	
SEEK FWD ↓	0	0	0	0	1	1	1	
	0	0	1	0	0	1	1	
	0	1	0	1	0	1	1	
	0	1	1	1	0	0	1	← PHASE A
↑ SEEK REV	1	0	0	1	1	0	1	
	1	0	1	1	1	0	0	
	1	1	0	1	1	1	0	
	1	1	1	0	1	1	0	

FIGURE 2. STEP TIMING

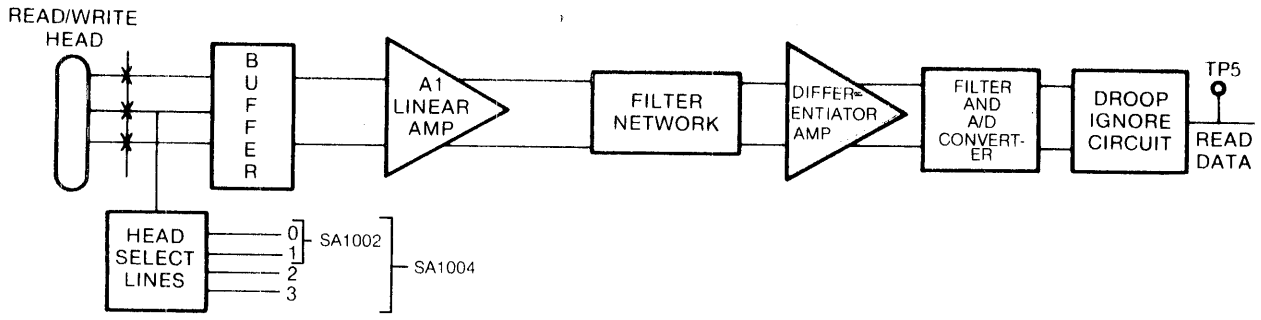


FIGURE 3. READ CHANNEL BLOCK DIAGRAM

2.5.2 NORMAL STEPPING

Normal seeking entails exactly the same sequence of events as the Buffered Step Mode with the only difference being that only one step pulse is loaded into the Step Buffer, and the rate of stepping is considerably slower. In this mode of operation the read/write heads will move at the rate of the incoming step pulses. The pulse width is 3μs minimum and the minimum time between successive steps is 1.5ms.

2.6 STEPPER DRIVER (CONTROL P.C.B.)

The stepper driver circuit is enabled by a low active enable step signal. The phase signals are entered via cable J9, and are gated through open collector type drivers. For discussion purposes, assume that phase A_2 is active, this signal would turn on Q18 and Q22 respectively, allowing the 24v Darlington switch to pass current through Q22 (low impedance), and to the A_2 coil phase of the stepper motor. The activated A_2 phase will also cause Q10 and Q27 to turn on. The amount of current flowing through the Phase A winding is regulated by a switching regulating circuit consisting of 5A2, 4B1, Q14 and Q16. The current is monitored at a summing node and at the voltage comparator 5A2. If the current becomes too high, comparator 5A2 will switch, turning off Q14 and Q16. This prevents any current from flowing through the phase A_2 motor coil. In this mode the 5A2 comparator will switch on and off as required. Transistors Q21 and Q28 are in the off mode providing a high impedance path for current to flow from Q21 into the A_1 phase winding. This prevents any other phases from becoming activated. Once the desired cylinder has been reached + REF seek complete will go true turning on Q29 and enabling + 5 volts to hold the stepper motor in position. The limiter 6A2 is activated and it regulates current flow to the motor coil.

2.7 READ (CONTROL PCB, REFER TO FIGURE 3)

In order to initiate a read operation the following conditions must be satisfied:

— A selected drive.

— Drive Ready Active.

— A selected head.

— Write gate inactive.

— All Fault conditions cleared.

— Seek complete.

The read operation begins with raw read data flowing through the selected head. Resistor R1 (430Ω) provides read damping necessary for the detection of flux transitions, and also provides the necessary impedance matching between the read/write head and the first amplification stage. The first stage of the read channel consists of isolation transistors Q2 and Q9, and protection diodes(CR9 and CR10). Differential amplifier 2F functions as a high pass filter allowing any frequency above 15 Khz to pass through, and the 4 pole Bessel filter acts as a low pass filter allowing only frequencies below 5.3 Mhz to pass through. Transistors Q3 and Q4 act as an active impedance matching network to the final stage of signal amplification. The final stage of amplification consists of a differential op amp, which allows only frequencies below 22 Mhz to pass. Typical amplification for the total read channel is 104 for 1F and 97 for 2F frequency. A 2 pole Bessel filter with a corner frequency at 3.3 Mhz is inserted between 3F and 5F for additional droop reduction. The amplified raw data is digitized by a zero crossover detect one shot (8T20). The delay created by the one shot at location 7B is used to delay erratic data long enough to be out of the window created by the combination of IC 7F and IC 6F11. The output of 6E3 (or TP 5) is the digitized droop ignore circuit (noise ignored). The digitized read data is then gated to the interface.

2.8 WRITE

In order to initiate a write operation the following conditions must be satisfied:

- Write gate on.
- Ready.
- Drive selected.
- Head selected.
- No fault conditions.
- Seek complete.

Assuming that the above conditions are satisfied a Write operation will be initiated. The write operation begins with an active Write gate signal at 4D9. Write Gate active will turn off the read detector, and turn on transistors Q6 and 2C8, 9, 10, allowing current to flow through the write current sense line. Current flow is limited by three 1% resistors R22, R23 and R24. If the cylinder is less than 128,Reduce IW signal should be in the inactive state, which allows an extra 10 ma to flow. When the cylinder count becomes greater than 128, Reduce IW should be activated, turning off transistor 2C12, 13, 14 preventing current from flowing through R22, thus reducing the amount of current by approximately 10 ma. Current flow is monitored by + IW Sense signal. This signal alerts the control circuitry that an Write operation is being performed. Write data is gated to F/F 5D, which divides the write data. In this mode write current will be switched by alternately turning 2C on and off. Write data will be written to the head whose center tap has been selected by the decoder IC (1C).

2.9 ERROR DETECTION (CONTROL P.C.B.)

The fault signal is used to inhibit improper writing on the disk. There are two basic fault conditions that are detected. They are:

1. Write Current in the heads wihtout Write Gate active.
2. Multiple heads selected.

Fault condition 1 will set latch 6D, preventing any data from being written on the disk. Fault condition 2 will also set latch 6D, indicating more than one head has been selected. In order to reset any fault condition the drive select line must be inactive for at least 500 ns or until a power-on-reset is applied.

Section 2

Maintenance

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1.0 TROUBLESHOOTING TECHNIQUES

1.1 PHILOSOPHY

The following troubleshooting techniques are designed to aid field service personnel in locating a drive fault down to the circuit level or to determine that the drive is not field repairable, in which case the drive must be repaired at a depot facility.

1.2 EQUIPMENT REQUIRED

1. A power supply capable of generating the following voltages:

   +5 volts @ 3.6 Amps
   -5 volts @ .2 Amp or (-7 to -16 VDC optional)
   +24 volts @ 2.8 Amps

2. Oscilloscope - Tektronix 465 or equivalent
   a. Probes: X 10 2 each
   X 1 1 each
   b. clip-on current probe

3. Digital Multimeter - H/P 3476B or equivalent.

1.3 PCB TEST POINTS

1.3.1 Control PCB Test Points

2	INDEX SIGNAL 19.2 ms (Fig. 4)
3	DIFFERENTIATED READ DATA
4	DIFFERENTIATED READ DATA
5	DIGITIZED READ DATA
6	TRACK 000 FLAG 1, LOGICAL 1 = TRK 000
7	WRITE GATE
8	ENABLE STEP (Fig. 5)
9	WRITE DATA MFM
10	SEEK COMPLETE
11	GROUND
(8F-9)	SYSTEM CLOCK 3.69μsec (Fig. 6)
12	READ DATA
14	GROUND
15	GROUND

1.3.2 Stepper PCB Test Points

1	STEP COMPLETE (LAST STEP)
2	GROUND
3	GROUND
5	STEP RATE SIGNAL

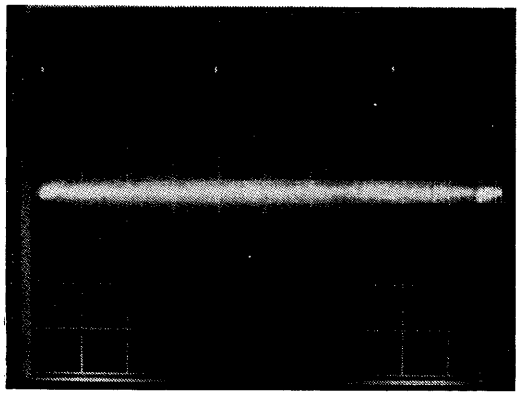


FIGURE 4. 2V/div 5 ms

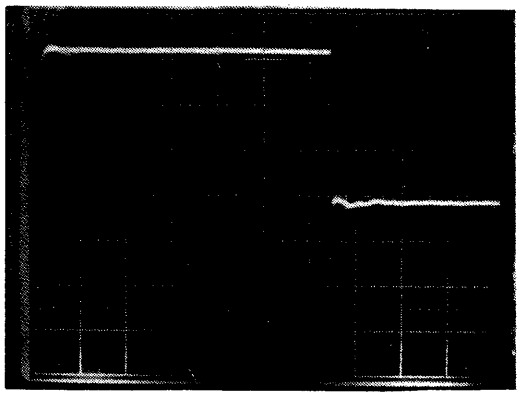


FIGURE 5. 2μs SEQUENCIAL SEEK 2V/DIV 2μS/DIV

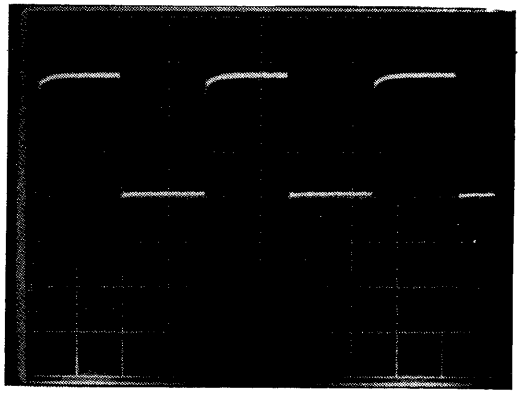


FIGURE 6. 2V/DIV 1μs

1.4 TROUBLESHOOTING FLOWCHARTS

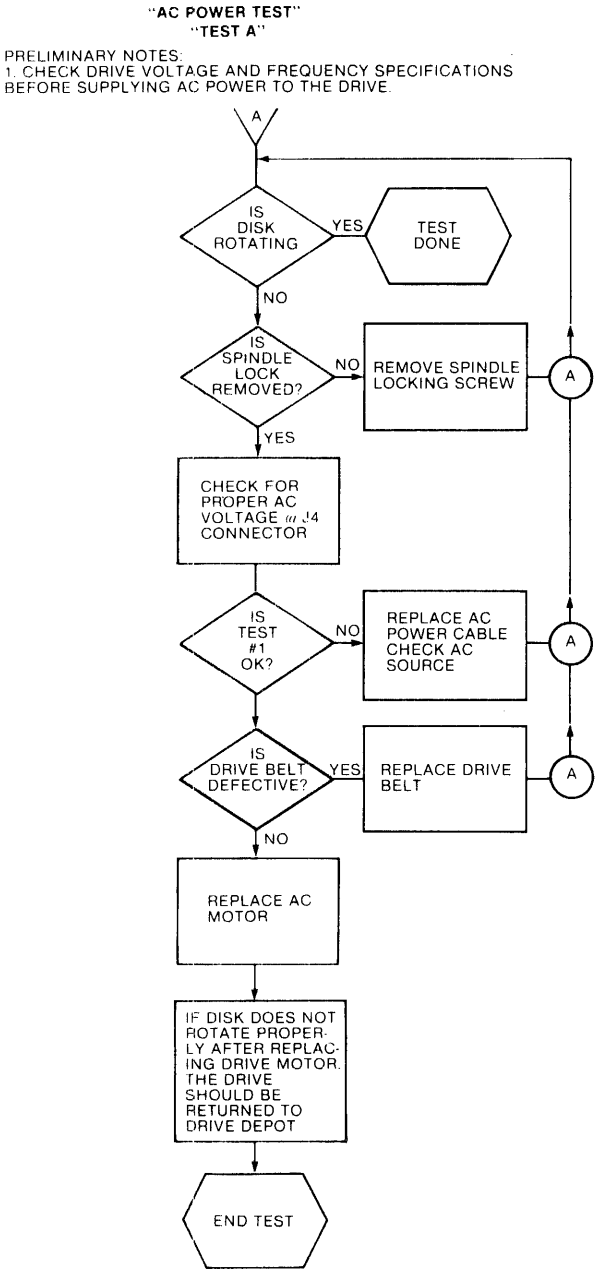
The interface signals utilized by various flowcharts may be generated by the host system/controller through its own diagnostic routines.

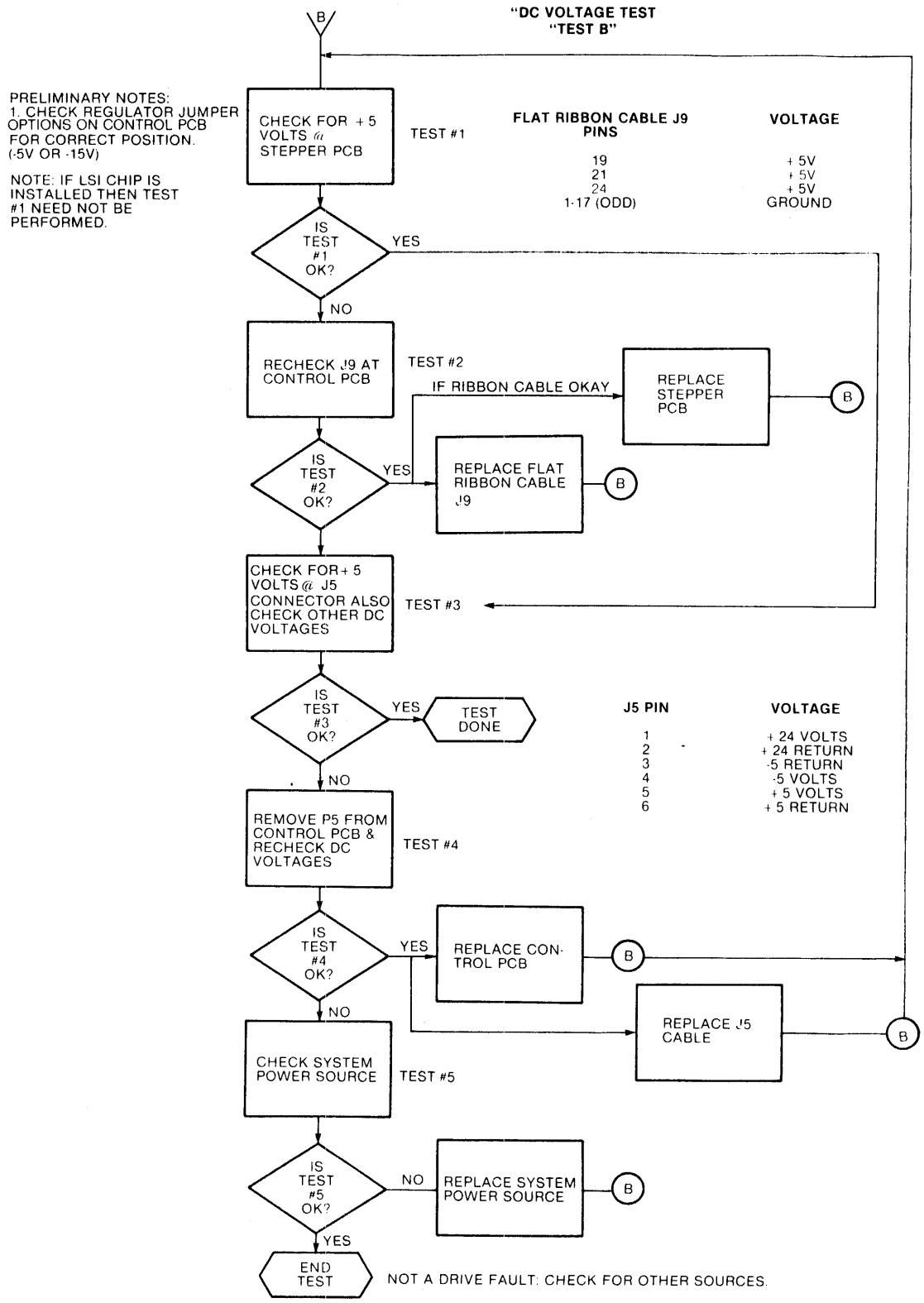
FLOW CHARTS

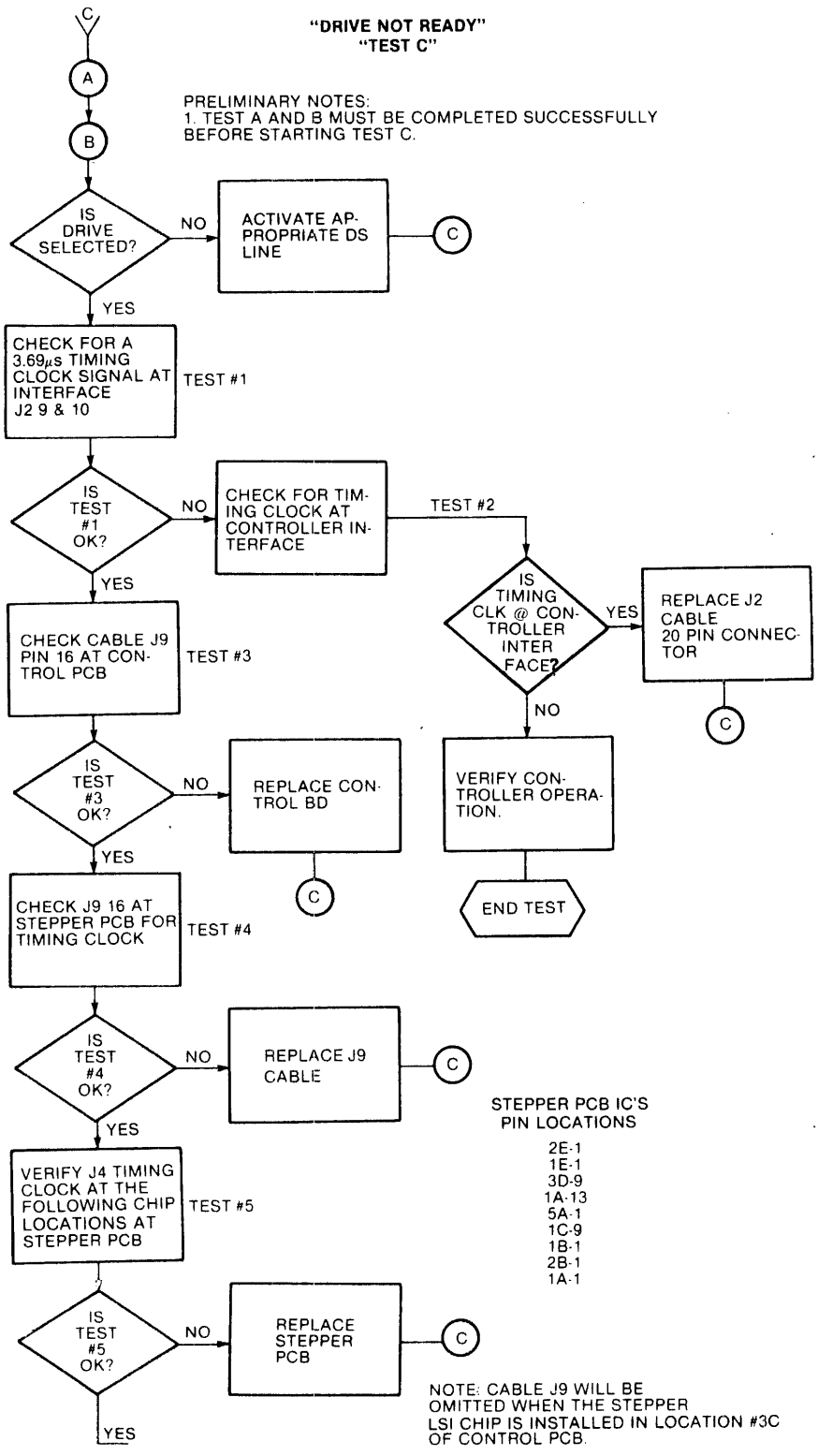
Test entry point

Perform test indicated

Test is completed successfully go to next test.

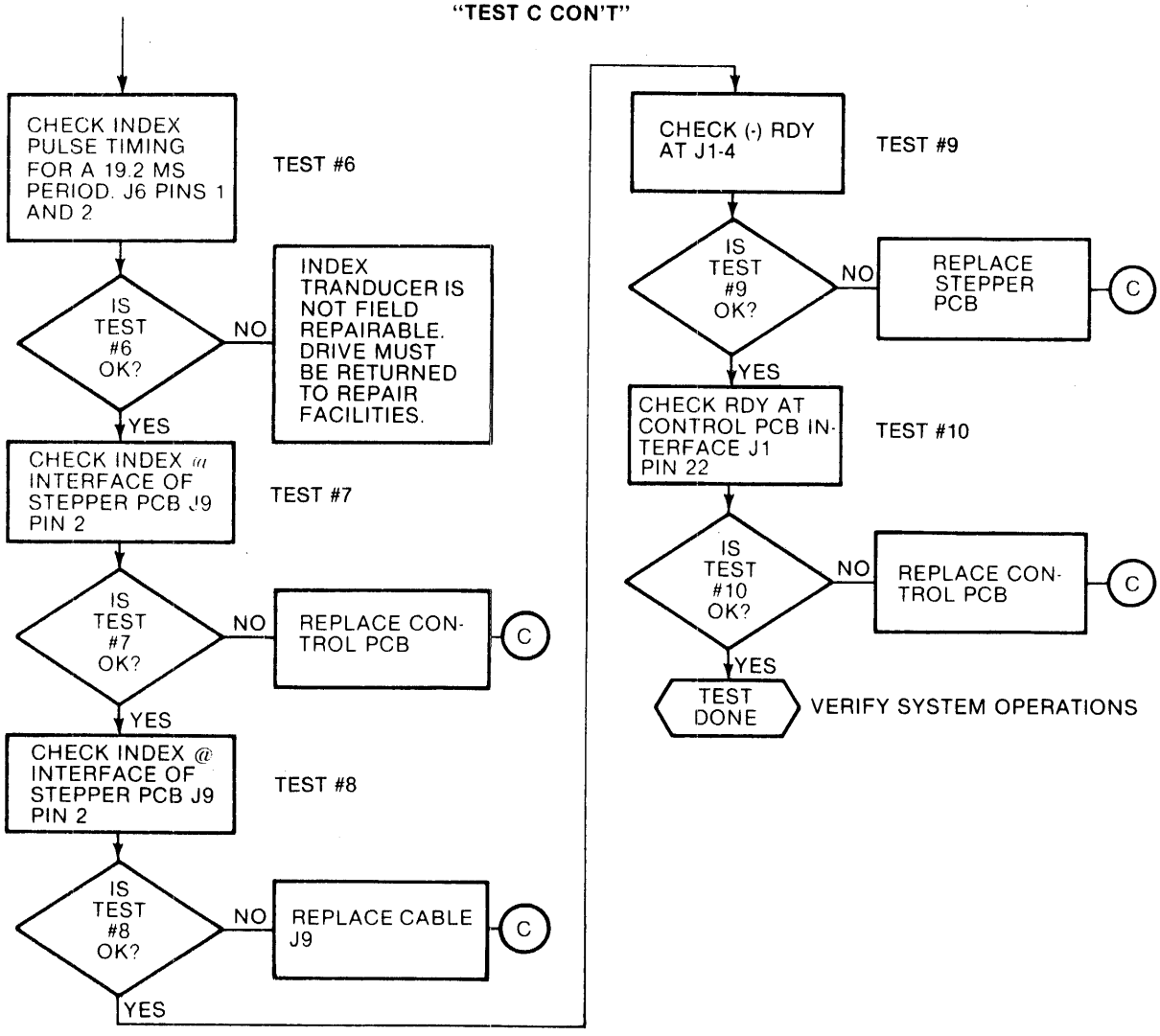


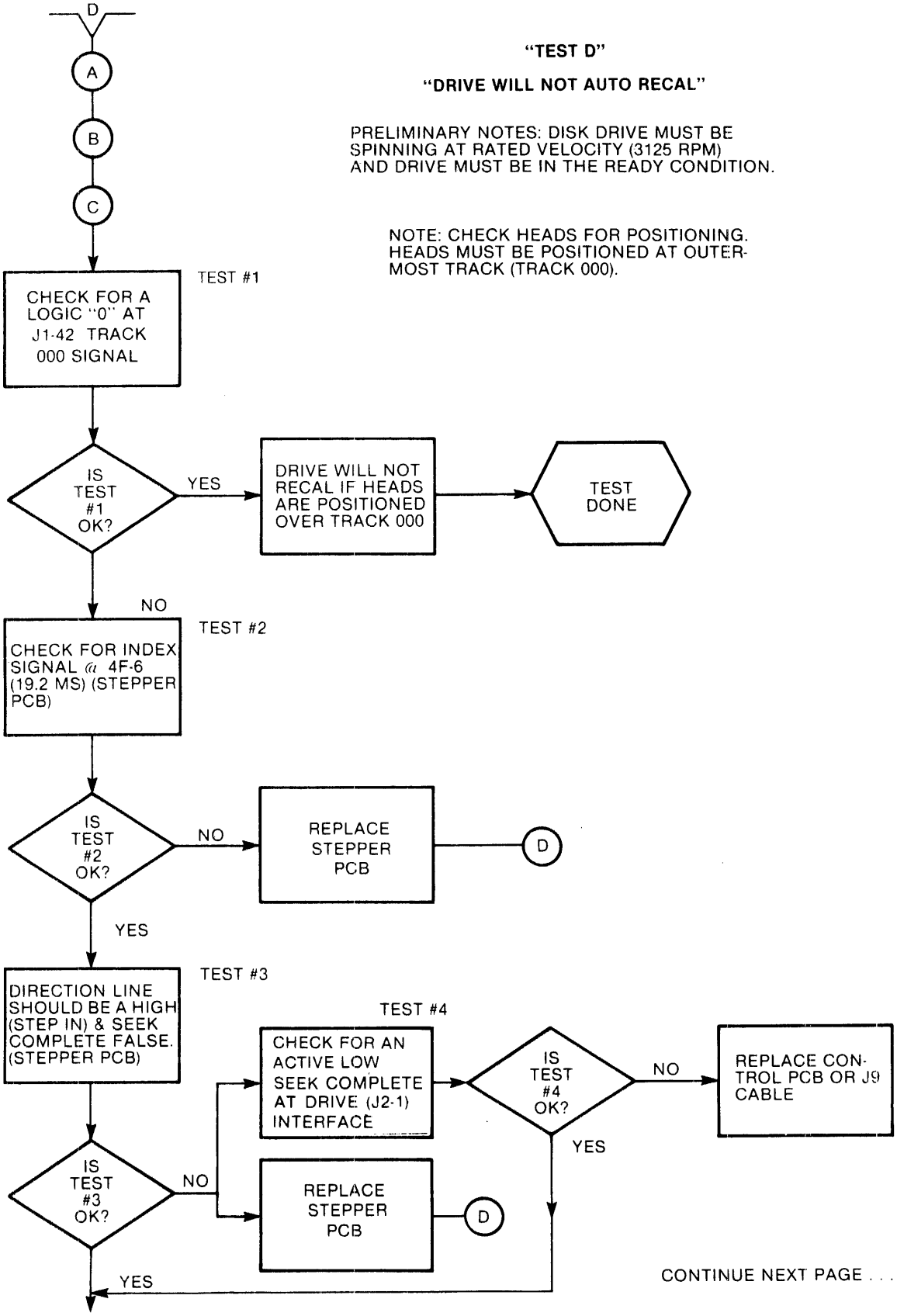

"DC VOLTAGE TEST
"TEST B"
B
PRELIMINARY NOTES:
1. CHECK REGULATOR JUMPER OPTIONS ON CONTROL PCB FOR CORRECT POSITION. (-5V OR -15V)
NOTE: IF LSI CHIP IS INSTALLED THEN TEST #1 NEED NOT BE PERFORMED.
CHECK FOR + 5 VOLTS @ STEPPER PCB
TEST #1
FLAT RIBBON CABLE J9 PINS
VOLTAGE
19 + 5V
21 + 5V
24 + 5V
1-17 (ODD) GROUND
IS TEST #1 OK?
YES
NO
RECHECK J9 AT CONTROL PCB
TEST #2
IF RIBBON CABLE OKAY
REPLACE STEPPER PCB
B
IS TEST #2 OK?
YES
REPLACE FLAT RIBBON CABLE J9
B
CHECK FOR+ 5 VOLTS @ J5 CONNECTOR ALSO CHECK OTHER DC VOLTAGES
TEST #3
IS TEST #3 OK?
YES
TEST DONE
J5 PIN
VOLTAGE
1 + 24 VOLTS
2 + 24 RETURN
3 -5 RETURN
4 -5 VOLTS
5 + 5 VOLTS
6 + 5 RETURN
NO
REMOVE P5 FROM CONTROL PCB & RECHECK DC VOLTAGES
TEST #4
IS TEST #4 OK?
YES
REPLACE CONTROL PCB
B
NO
REPLACE J5 CABLE
B
CHECK SYSTEM POWER SOURCE
TEST #5
IS TEST #5 OK?
NO
REPLACE SYSTEM POWER SOURCE
B
YES
END TEST
NOT A DRIVE FAULT: CHECK FOR OTHER SOURCES.



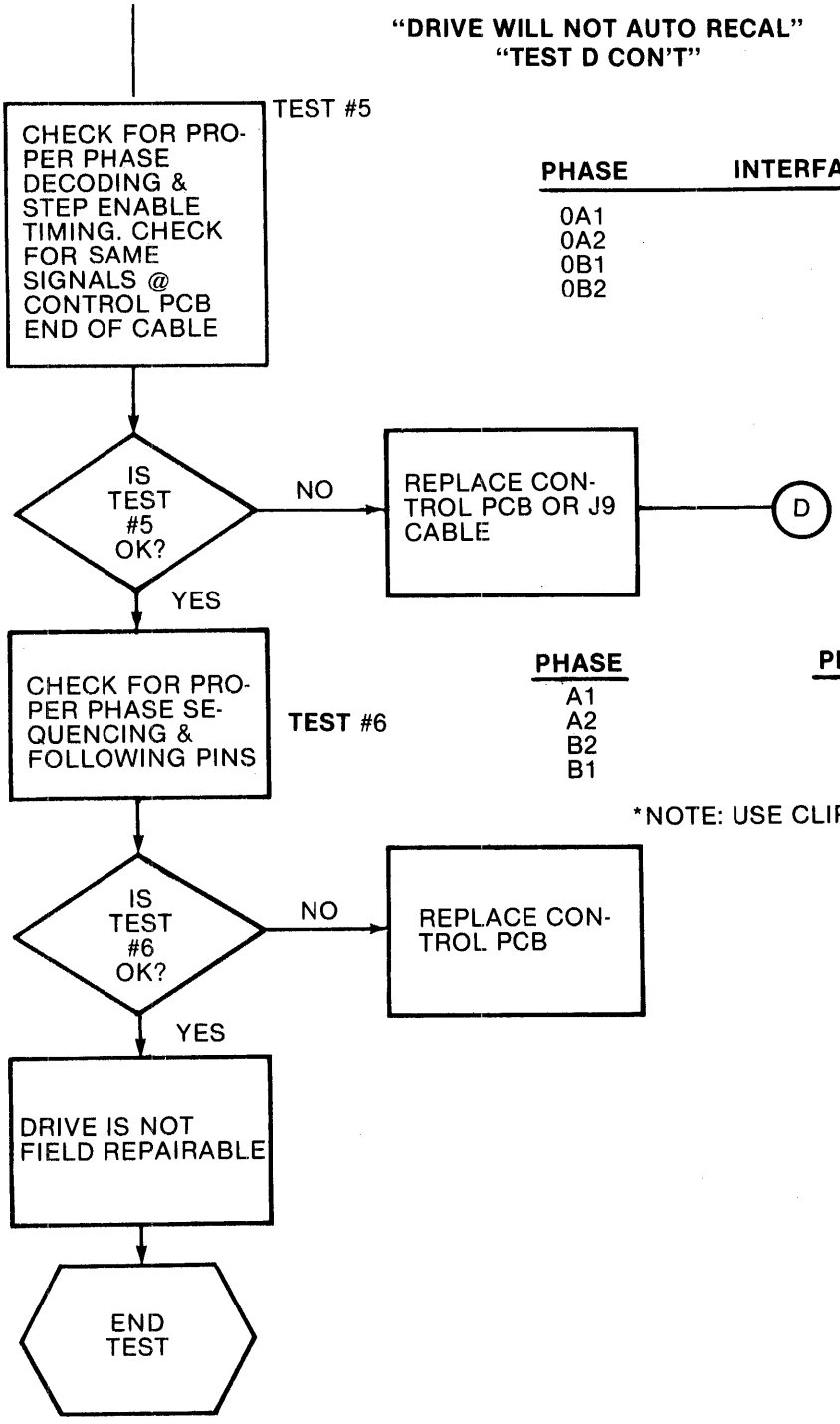
TEST C CONTINUED NEXT PAGE

"DRIVE NOT READY"
"TEST C CON'T"




D
A
B
C
"TEST D"
"DRIVE WILL NOT AUTO RECAL"
PRELIMINARY NOTES: DISK DRIVE MUST BE SPINNING AT RATED VELOCITY (3125 RPM) AND DRIVE MUST BE IN THE READY CONDITION.
NOTE: CHECK HEADS FOR POSITIONING. HEADS MUST BE POSITIONED AT OUTER-MOST TRACK (TRACK 000).
TEST #1
CHECK FOR A LOGIC "0" AT J1-42 TRACK 000 SIGNAL
IS TEST #1 OK?
YES
DRIVE WILL NOT RECAL IF HEADS ARE POSITIONED OVER TRACK 000
TEST DONE
NO
TEST #2
CHECK FOR INDEX SIGNAL @ 4F-6 (19.2 MS) (STEPPER PCB)
IS TEST #2 OK?
NO
REPLACE STEPPER PCB
D
YES
TEST #3
DIRECTION LINE SHOULD BE A HIGH (STEP IN) & SEEK COMPLETE FALSE. (STEPPER PCB)
TEST #4
CHECK FOR AN ACTIVE LOW SEEK COMPLETE AT DRIVE (J2-1) INTERFACE
IS TEST #4 OK?
NO
REPLACE CONTROL PCB OR J9 CABLE
YES
IS TEST #3 OK?
NO
REPLACE STEPPER PCB
D
YES
CONTINUE NEXT PAGE . . .

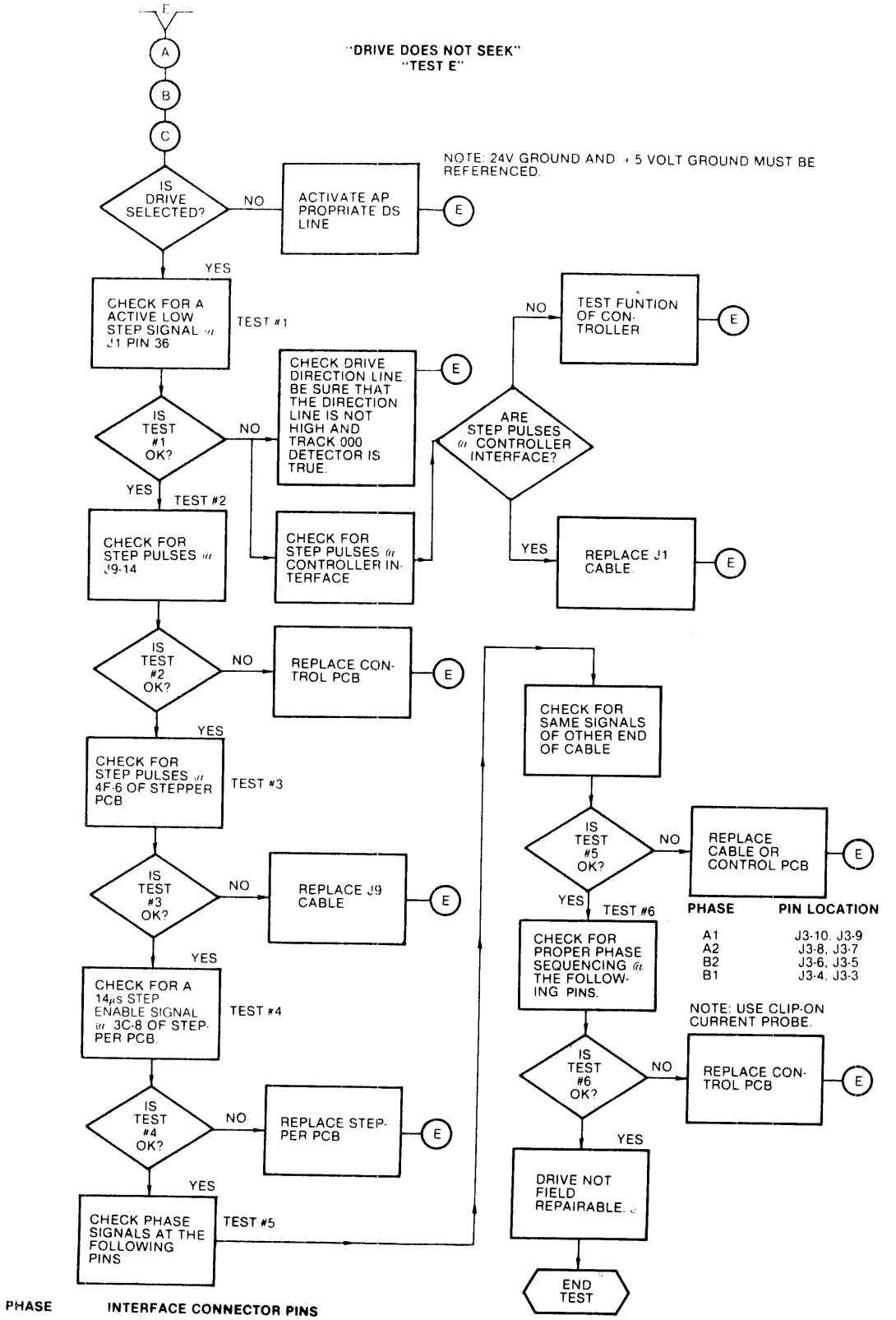
"DRIVE WILL NOT AUTO RECAL"
"TEST D CON'T"

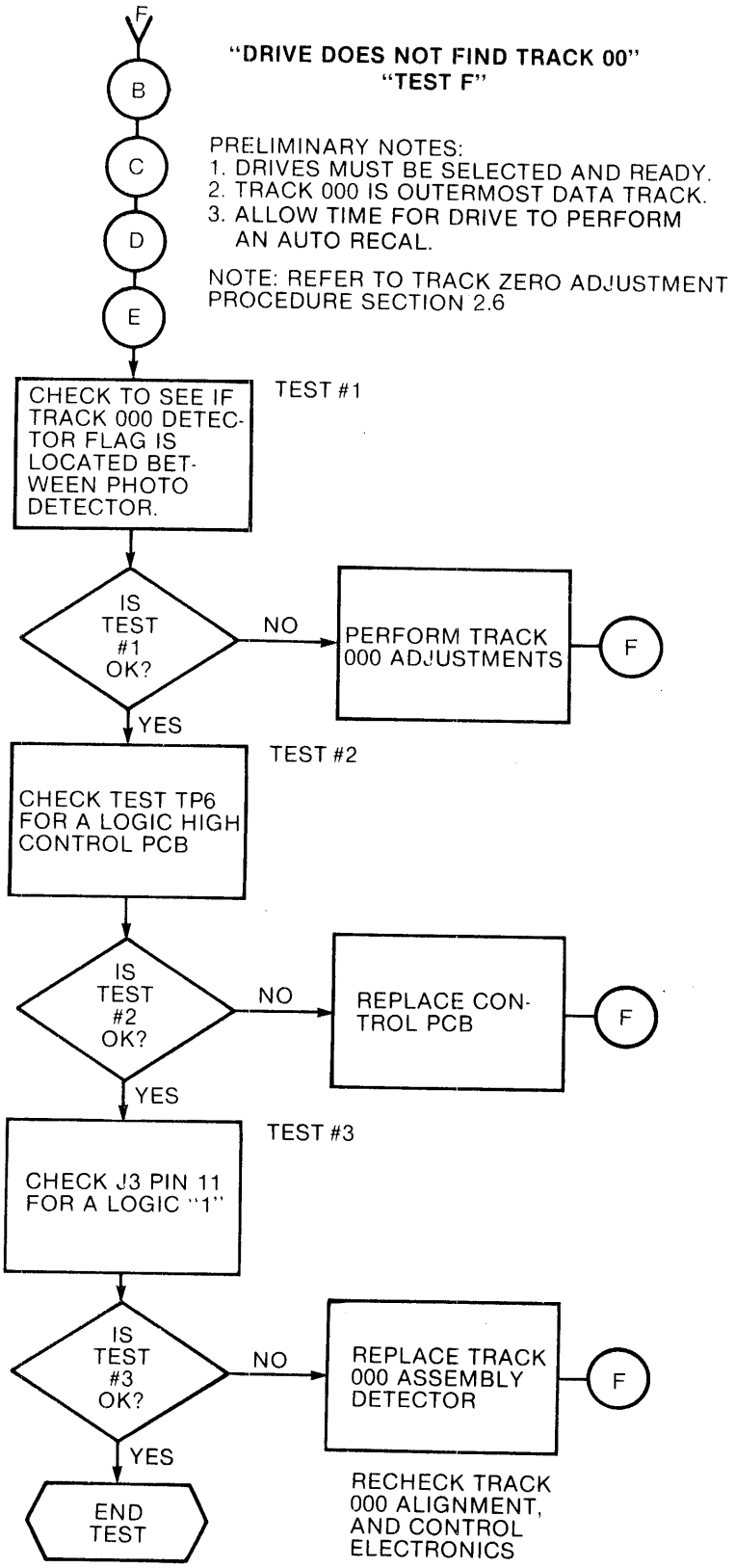


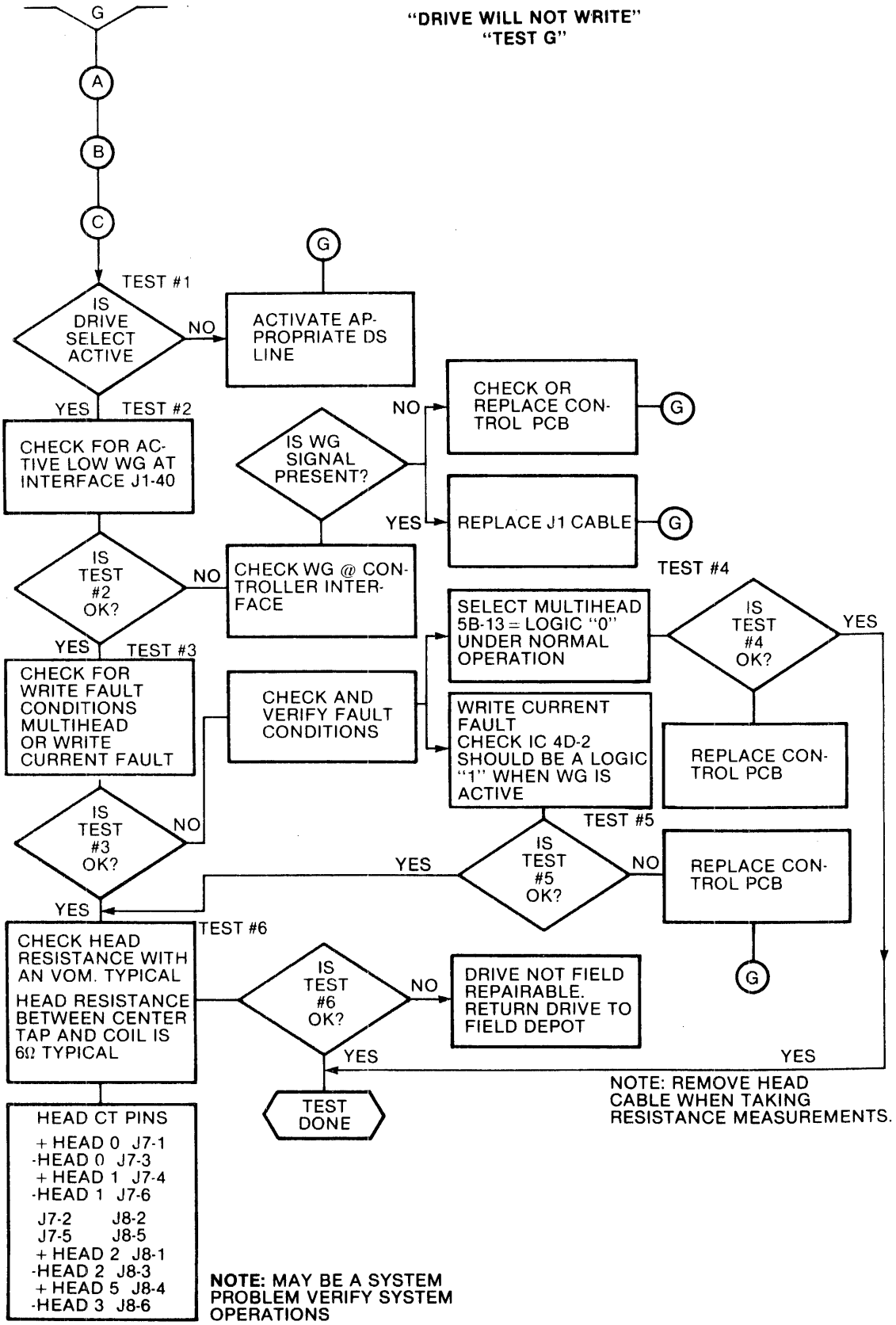
PHASE	INTERFACE CONNECTOR PCB
0A1	22
0A2	23
0B1	26
0B2	25

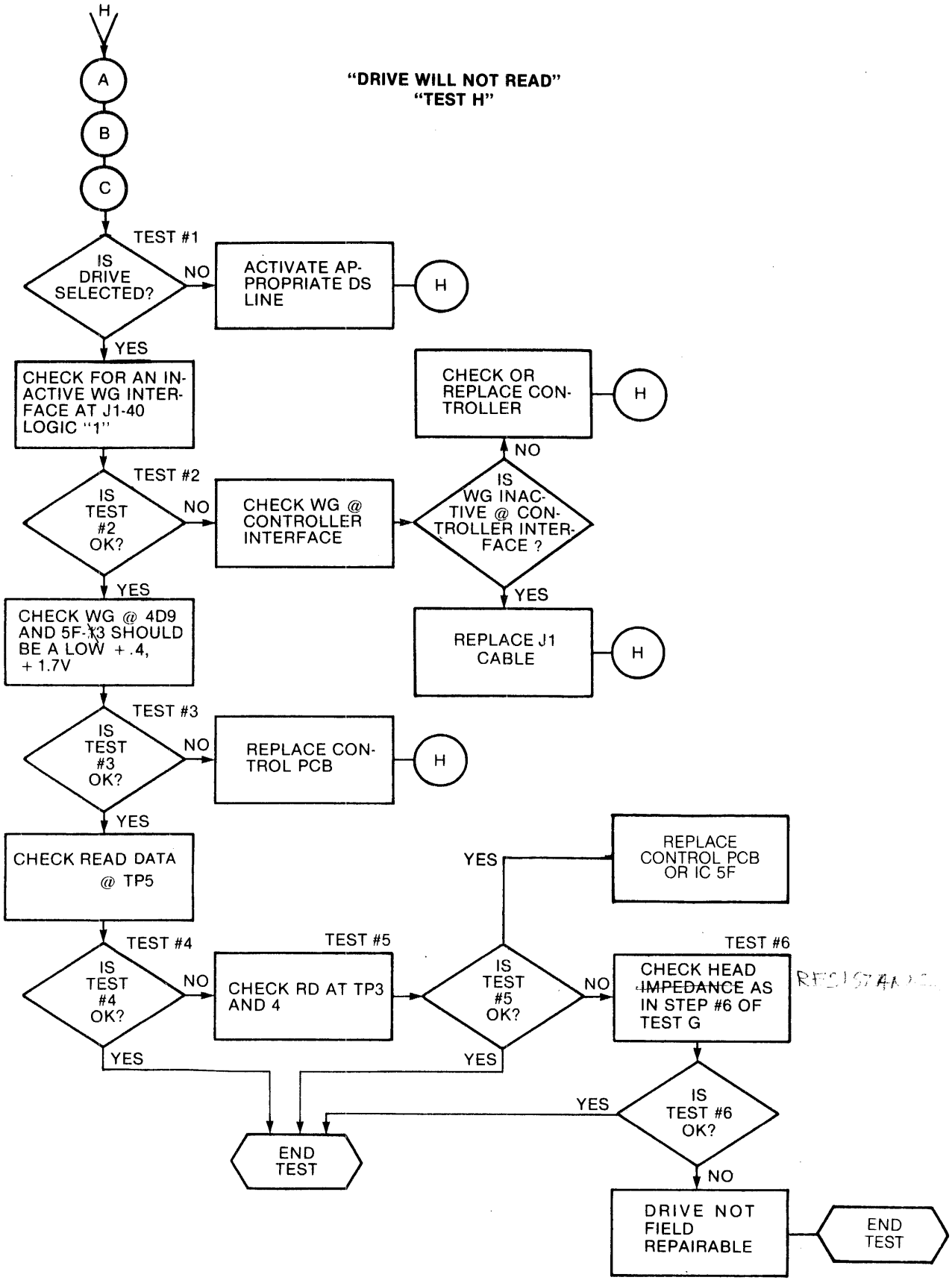
PHASE	PIN LOCATIONS
A1	J3-10 & J3-9
A2	J3-8 & J3-7
B2	J3-6 & J3-5
B1	J3-4 & J3-3

*NOTE: USE CLIP ON CURRENT PROBE


"DRIVE DOES NOT SEEK"
"TEST E"
NOTE: 24V GROUND AND + 5 VOLT GROUND MUST BE REFERENCED.
IS DRIVE SELECTED?
NO
ACTIVATE APPROPRIATE DS LINE
YES
CHECK FOR A ACTIVE LOW STEP SIGNAL @ J1 PIN 36
TEST #1
IS TEST #1 OK?
NO
CHECK DRIVE DIRECTION LINE. BE SURE THAT THE DIRECTION LINE IS NOT HIGH AND TRACK 000 DETECTOR IS TRUE.
YES
TEST #2
CHECK FOR STEP PULSES @ J9-14
CHECK FOR STEP PULSES @ CONTROLLER INTERFACE
ARE STEP PULSES @ CONTROLLER INTERFACE?
NO
TEST FUNTION OF CONTROLLER
YES
REPLACE J1 CABLE.
IS TEST #2 OK?
NO
REPLACE CONTROL PCB
YES
CHECK FOR STEP PULSES @ 4F-6 OF STEPPER PCB
TEST #3
IS TEST #3 OK?
NO
REPLACE J9 CABLE
YES
CHECK FOR A 14μS STEP ENABLE SIGNAL @ 3C-8 OF STEPPER PCB.
TEST #4
IS TEST #4 OK?
NO
REPLACE STEPPER PCB
YES
CHECK PHASE SIGNALS AT THE FOLLOWING PINS
TEST #5
CHECK FOR SAME SIGNALS OF OTHER END OF CABLE
IS TEST #5 OK?
NO
REPLACE CABLE OR CONTROL PCB
YES
TEST #6
CHECK FOR PROPER PHASE SEQUENCING @ THE FOLLOWING PINS.
PHASE
PIN LOCATION
A1 J3-10, J3-9
A2 J3-8, J3-7
B2 J3-6, J3-5
B1 J3-4, J3-3
NOTE: USE CLIP-ON CURRENT PROBE.
IS TEST #6 OK?
NO
REPLACE CONTROL PCB
YES
DRIVE NOT FIELD REPAIRABLE.
END TEST
PHASE
INTERFACE CONNECTOR PINS
0A1 22
0A2 23
0B1 26
0B2 25
NOTE B: IF DRIVE SEEKS, BUT GETS EXCESSIVE SEEK ERRORS, TRY REPLACING DAMPER ASSEMBLY REFER TO SECTION 2.4 FOR REPLACEMENT PROCEDURE.


F
B
C
D
E
"DRIVE DOES NOT FIND TRACK 00"
"TEST F"
PRELIMINARY NOTES:
1. DRIVES MUST BE SELECTED AND READY.
2. TRACK 000 IS OUTERMOST DATA TRACK.
3. ALLOW TIME FOR DRIVE TO PERFORM AN AUTO RECAL.
NOTE: REFER TO TRACK ZERO ADJUSTMENT PROCEDURE SECTION 2.6
CHECK TO SEE IF TRACK 000 DETECTOR FLAG IS LOCATED BETWEEN PHOTO DETECTOR.
TEST #1
IS TEST #1 OK?
NO
PERFORM TRACK 000 ADJUSTMENTS
F
YES
CHECK TEST TP6 FOR A LOGIC HIGH CONTROL PCB
TEST #2
IS TEST #2 OK?
NO
REPLACE CONTROL PCB
F
YES
CHECK J3 PIN 11 FOR A LOGIC "1"
TEST #3
IS TEST #3 OK?
NO
REPLACE TRACK 000 ASSEMBLY DETECTOR
F
YES
END TEST
RECHECK TRACK 000 ALIGNMENT, AND CONTROL ELECTRONICS


"DRIVE WILL NOT WRITE"
"TEST G"
G
A
B
C
TEST #1
IS DRIVE SELECT ACTIVE
NO
ACTIVATE APPROPRIATE DS LINE
G
YES
TEST #2
CHECK FOR ACTIVE LOW WG AT INTERFACE J1-40
IS WG SIGNAL PRESENT?
NO
CHECK OR REPLACE CONTROL PCB
G
YES
REPLACE J1 CABLE
G
IS TEST #2 OK?
NO
CHECK WG @ CONTROLLER INTERFACE
YES
TEST #3
CHECK FOR WRITE FAULT CONDITIONS MULTIHEAD OR WRITE CURRENT FAULT
CHECK AND VERIFY FAULT CONDITIONS
SELECT MULTIHEAD 5B-13 = LOGIC "0" UNDER NORMAL OPERATION
WRITE CURRENT FAULT CHECK IC 4D-2 SHOULD BE A LOGIC "1" WHEN WG IS ACTIVE
TEST #4
IS TEST #4 OK?
YES
REPLACE CONTROL PCB
IS TEST #3 OK?
NO
TEST #5
IS TEST #5 OK?
YES
NO
REPLACE CONTROL PCB
G
YES
TEST #6
CHECK HEAD RESISTANCE WITH AN VOM. TYPICAL
HEAD RESISTANCE BETWEEN CENTER TAP AND COIL IS 6Ω TYPICAL
IS TEST #6 OK?
NO
DRIVE NOT FIELD REPAIRABLE. RETURN DRIVE TO FIELD DEPOT
YES
YES
TEST DONE
NOTE: REMOVE HEAD CABLE WHEN TAKING RESISTANCE MEASUREMENTS.
HEAD CT PINS
+HEAD 0 J7-1
-HEAD 0 J7-3
+HEAD 1 J7-4
-HEAD 1 J7-6
J7-2 J8-2
J7-5 J8-5
+HEAD 2 J8-1
-HEAD 2 J8-3
+HEAD 5 J8-4
-HEAD 3 J8-6
NOTE: MAY BE A SYSTEM PROBLEM VERIFY SYSTEM OPERATIONS


H
A
B
C
"DRIVE WILL NOT READ"
"TEST H"
TEST #1
IS DRIVE SELECTED?
NO
ACTIVATE APPROPRIATE DS LINE
H
YES
CHECK FOR AN INACTIVE WG INTERFACE AT J1-40 LOGIC "1"
CHECK OR REPLACE CONTROLLER
H
NO
TEST #2
IS TEST #2 OK?
NO
CHECK WG @ CONTROLLER INTERFACE
IS WG INACTIVE @ CONTROLLER INTERFACE ?
YES
YES
CHECK WG @ 4D9 AND 5F-13 SHOULD BE A LOW + .4, + 1.7V
REPLACE J1 CABLE
H
TEST #3
IS TEST #3 OK?
NO
REPLACE CONTROL PCB
H
YES
CHECK READ DATA @ TP5
YES
REPLACE CONTROL PCB OR IC 5F
TEST #4
IS TEST #4 OK?
NO
TEST #5
CHECK RD AT TP3 AND 4
IS TEST #5 OK?
NO
TEST #6
CHECK HEAD IMPEDANCE AS IN STEP #6 OF TEST G
YES
YES
YES
IS TEST #6 OK?
END TEST
NO
DRIVE NOT FIELD REPAIRABLE
END TEST

2.0 DRIVE MOTOR/PULLEY/BELT REMOVAL INSTRUCTIONS

1. Remove the connectors at J5, J6, J7, J8 and J9, on the control PCB.
2. Unfasten the four keyed PCB mounts.
3. Remove the PCB.
4. Unscrew the three cover mounting nuts (refer to Fig. 7).
5. Remove the cover.

REFERENCE FIGURE 8 FOR THE FOLLOWING

6. Remove the drive motor belt (60Hz — P/N 60375; 50Hz — P/N 60376) by rotating the spindle clockwise. **CAUTION:** Counter-clockwise rotation may damage the heads or media.
7. Loosen the two allen head set screws on the drive motor pulley and remove it from the drive motor shaft.
8. Loosen the screw that secures the capacitor mounting bracket to the casting and rotate the bracket clear of the capacitor.
9. Release the AC connector plug from its bracket on the casting.
10. Note the location of the three wires on the capacitor and remove them.
11. Unfasten the four locknuts securing the drive motor. Remove the four insulated washers and ground strap. The motor may now be withdrawn from the drive.

2.1 DRIVE MOTOR/PULLEY/BELT INSTALLATION INSTRUCTIONS

1. Verify that there is an insulated washer (P/N 60482) on each of the four drive motor mounting shafts.
2. Locate the motor in its cavity in the base casting and install four more insulated washers. Install the four locknuts, leaving them slightly loose.
3. Measure the center-to-center distance from the spindle shaft to the drive motor shaft. This distance must be 7.73 inches. Reposition the drive motor if necessary. Tighten the locknuts securely. **CAUTION:** Counter-clockwise rotation may damage the heads or media.
4. Route the AC connector plug leads between the capacitor and the base casting. Insert the plug into its bracket.
5. Reconnect the three capacitor wires and tighten the capacitor bracket mounting screw.
6. Install the drive motor pulley on the drive motor shaft so that there is .660 inch clearance between the top edge of the pulley and the drive motor face (refer to Fig. 8a). Insure that one of the set screws is located on the flat side of the drive motor shaft. Tighten the screws.
7. Reinstall the control PCB.
8. Reinstall the cover and secure with the three mounting washers and nuts.

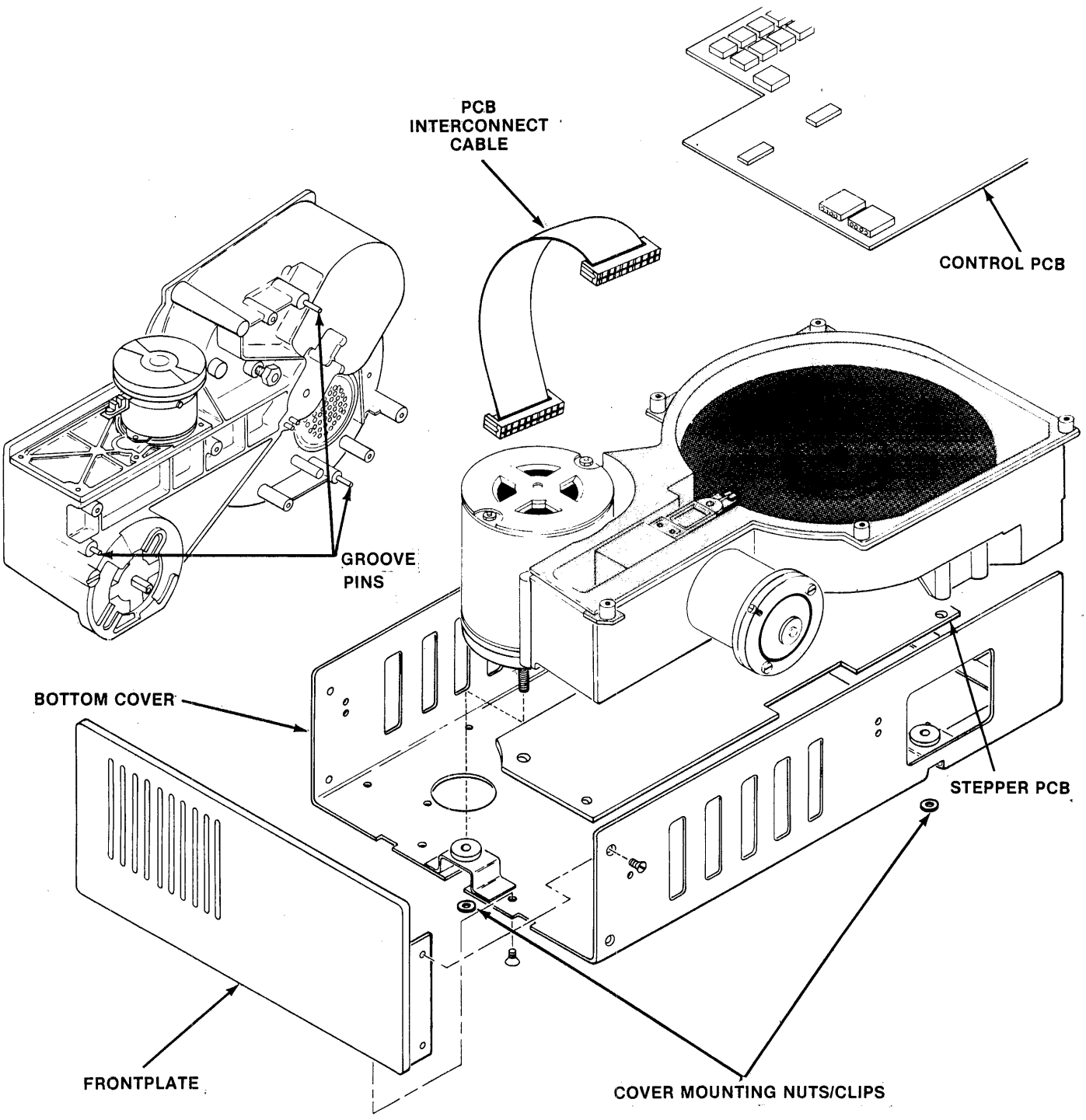


FIGURE 7. SA1000 COVER

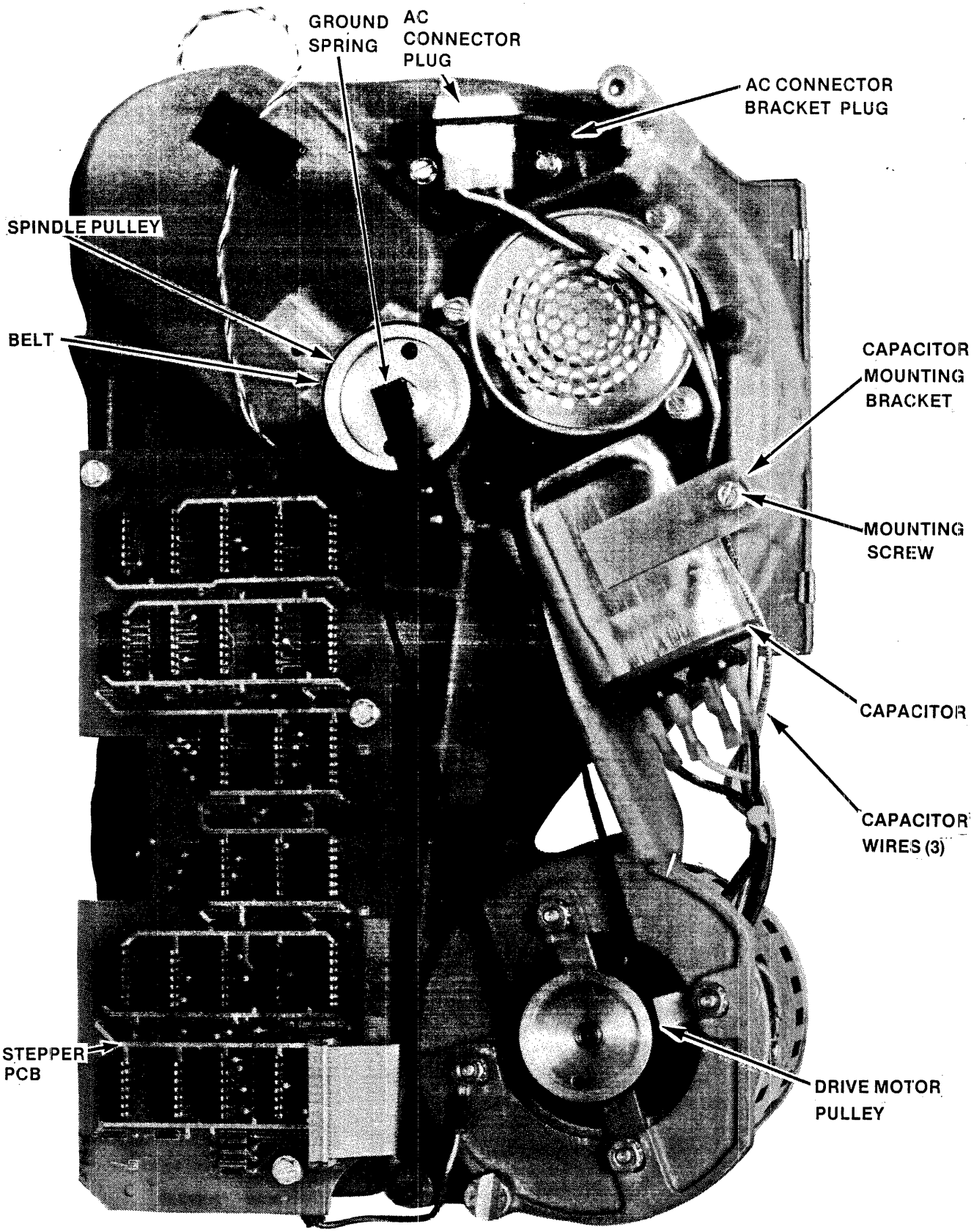


FIGURE 8. SA1000

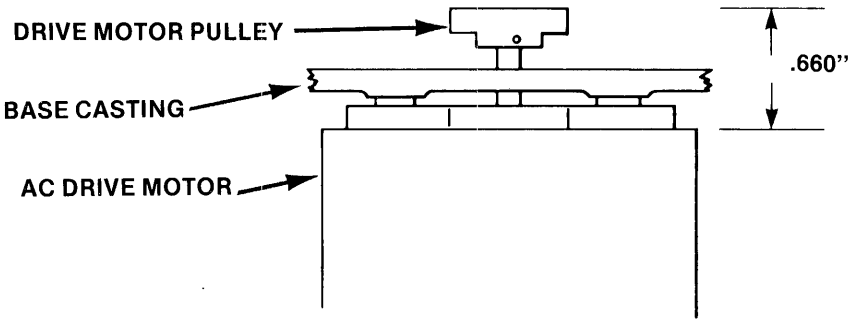


FIGURE 8a. DRIVE MOTOR PULLEY ADJUSTMENT

2.2 SPECIAL EQUIPMENT

A. 465 Tektronic scope or equivalent.

B. 1 × 10 probe.

2.3 INDEX TRANSDUCER ADJUSTMENT PROCEDURE

A. Remove the J6 cable from the control board.

B. Remove the cover assembly by unfastening the three mounting nuts.

C. Remove the stepper board.

D. Apply A/C power to the drive.

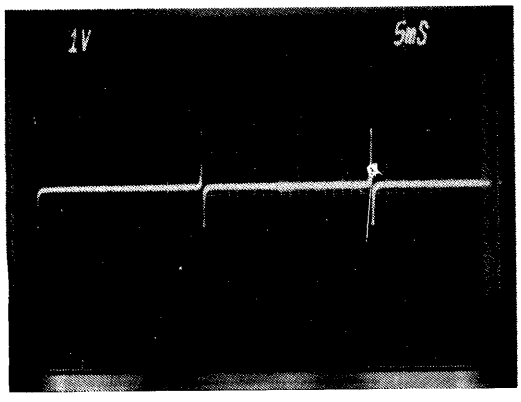
E. Place scope probe on signal wire of J6 cable, and ground the other side of J6 cable wire. (Mode AQ 1V/div, time base 5 ms).

F. Adjust the index transducer by turning the base with a 3/8'' open end wrench. Adjust the index pulse so that a .9V pp ± 0.1V pp minimum signal appears on the scope (see Figure 9).

G. Remove A/C power from drive.

H. Remount the stepper PCB and reinstall the index transducer cable to J6.

I. Reinstall the cover assembly.



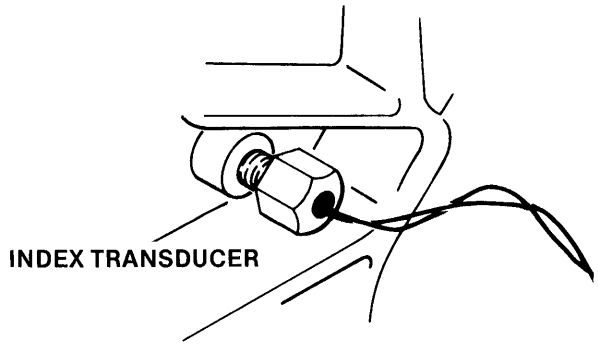


FIGURE 9. INDEX PULSE

2.4 DAMPER REMOVAL/INSTALLATION PROCEDURE

2.4.1 DAMPER REMOVAL PROCEDURE

A. Remove the filler screw from the side of damper (refer to Figure 10).

B. Insert a .050" allen wrench into the hole formerly occupied by the filler screw, and loosen the allen screw inside. Gently remove damper assembly by applying a light upward pressure. **NOTE:** The damper must remain upright to prevent fluid loss.

C. Reinstall filler screw.

D. Wipe damper clean.

2.4.2 DAMPER INSTALLATION PROCEDURE

A. Obtain new damper assembly, P/N 60477.

B. Apply A/C power to the drive.

C. Remove the cover screw from the side of the damper.

D. Insert an allen wrench into the cover screw hole and loosen the screw enough to slide the damper onto the actuator motor shaft.

E. Obtain the damper spacing tool (P/N 600548). Place the spacing tool between the damper and the track 000 clamp (see Fig. 11). Slide the damper against the tool and tighten the allen screw. Reinstall the filler screw.

F. Remove the spacing tool and wipe the damper clean.

G. Turn off AC power.

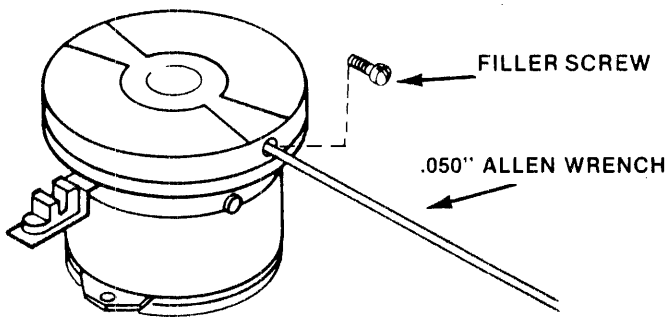


FIGURE 10. DAMPER REMOVAL

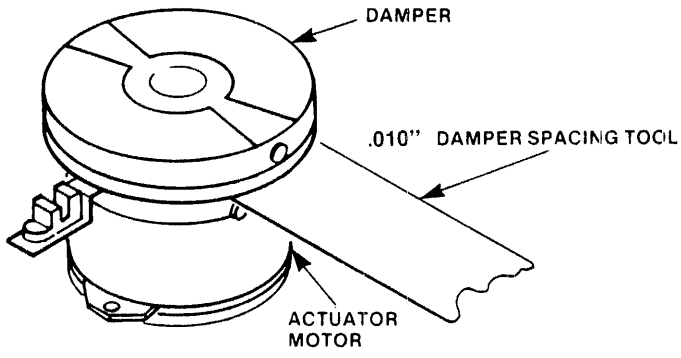


FIGURE 11. DAMPER INSTALLATION

2.5 TRACK 000 FLAG ASSEMBLY INSTALLATION AND REMOVAL

2.5.1 TRACK 000 FLAG ASSEMBLY REMOVAL

A. Apply AC/DC power.

B. Allow the drive to perform an auto recal.

C. Turn off DC power.

D. Remove the damper in order to access the flag assembly (P/N 60404). Reference Section 2.4.1, Damper Removal Procedure. **NOTE:** Caution should be used to insure that the actuator motor shaft does not move during this procedure.

E. Loosen the allen head set screw on the Track 000 flag collar (P/N 60417) (ref. Fig. 12).

F. Gently slide the collar off the actuator motor shaft.

2.5.2 TRACK 000 FLAG ASSEMBLY INSTALLATION

A. Install the flag assembly onto the actuator motor shaft. **NOTE:** Caution should be used to insure that the actuator motor shaft does not move during this procedure.

B. Locate the damper spacing tool (P/N 60548) between the top of the actuator motor and the bottom of the Track 000 flag collar (ref. Fig. 13).

C. Position the flag so that it is centered in the Track 000 detector assembly (ref. Fig. 14).

D. Tighten the set screw in the collar, verifying that the .010 inch gap remains when the spacing tool is removed.

E. Reinstall the damper assembly, as per Section 2.4.2.

2.6 TRACK 000 ADJUSTMENT PROCEDURE

2.6.1 TRACK ZERO ALIGNMENT PROCEDURE

A. Turn AC/DC power on.

B. Allow the drive to perform an auto recal.

C. Using an allen wrench, loosen the Track 000 clamp. (Insure that the clamp does not slip down on the actuator shaft).

D. With the drive at track zero, center Track 000 indicator flag in the center of Track 000 detector assembly (ref. Fig. 14).

E. Power down D.C. voltage.

F. Turn the damper counter-clockwise until it contacts the Track 000 crash stop.

G. Turn on D.C. voltage. The Track 000 flag should move 1/8'' while still maintaining center position.

H. Check TP6 on the control PCB for Track 000 indication (logical ''1'').

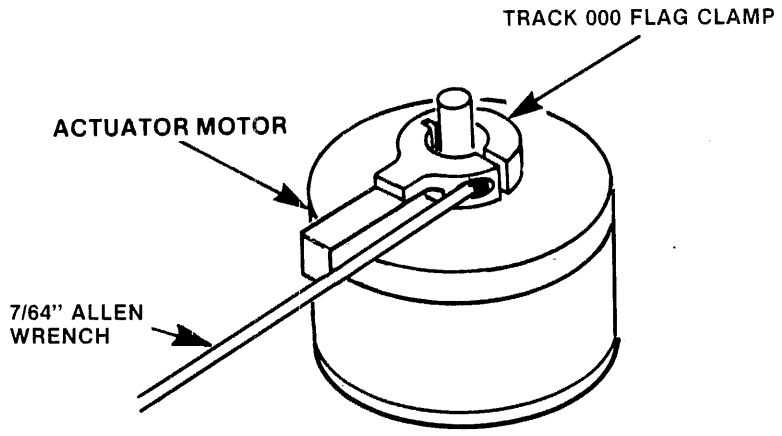


FIGURE 12. TRACK 000 FLAG COLLAR

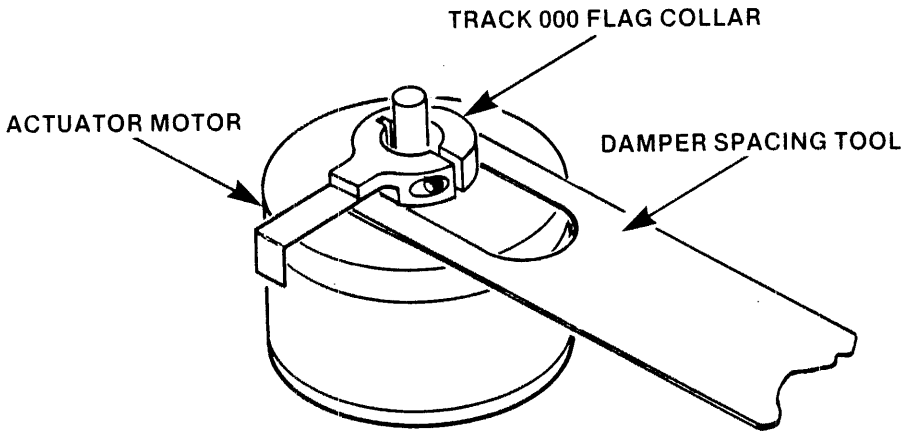


FIGURE 13. TRACK 000 FLAG ADJUSTMENT

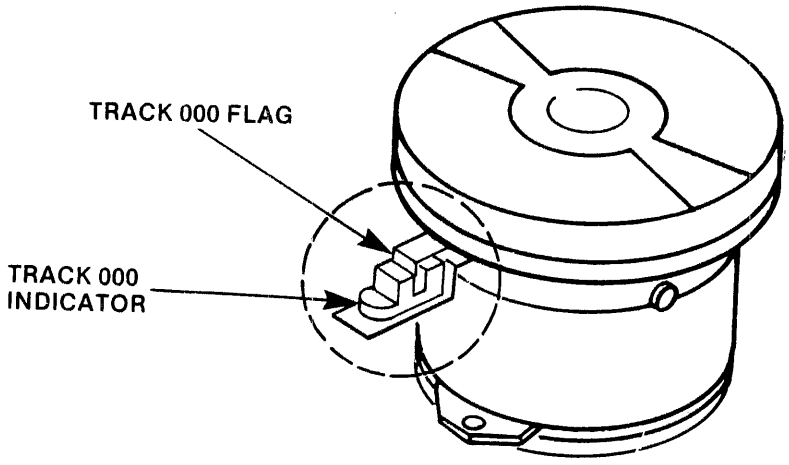


FIGURE 14. TRACK 000 FLAG ALIGNMENT

3.0 SA1000 JUMPER OPTIONS

The following jumper options are located on the control PCB, P/N 26050. Reference Figure 15 for the locations.

JUMPER	FUNCTION
Fault	When jumpered, this option disables the fault detection circuitry.
Ready	When jumpered, this option enables an active ready signal at the interface.
Drive Select (DS1 - 4)	When jumpered, this option selects the designated drive.
-5, -15 Volts	When jumpered in the -5 volt configuration, this option bypasses the regulator chip - to be used when the input voltage is rated at -5 volts. When jumpered in the -15 volt configuration, this option allows a -15 volt input to be regulated to -5 volts.

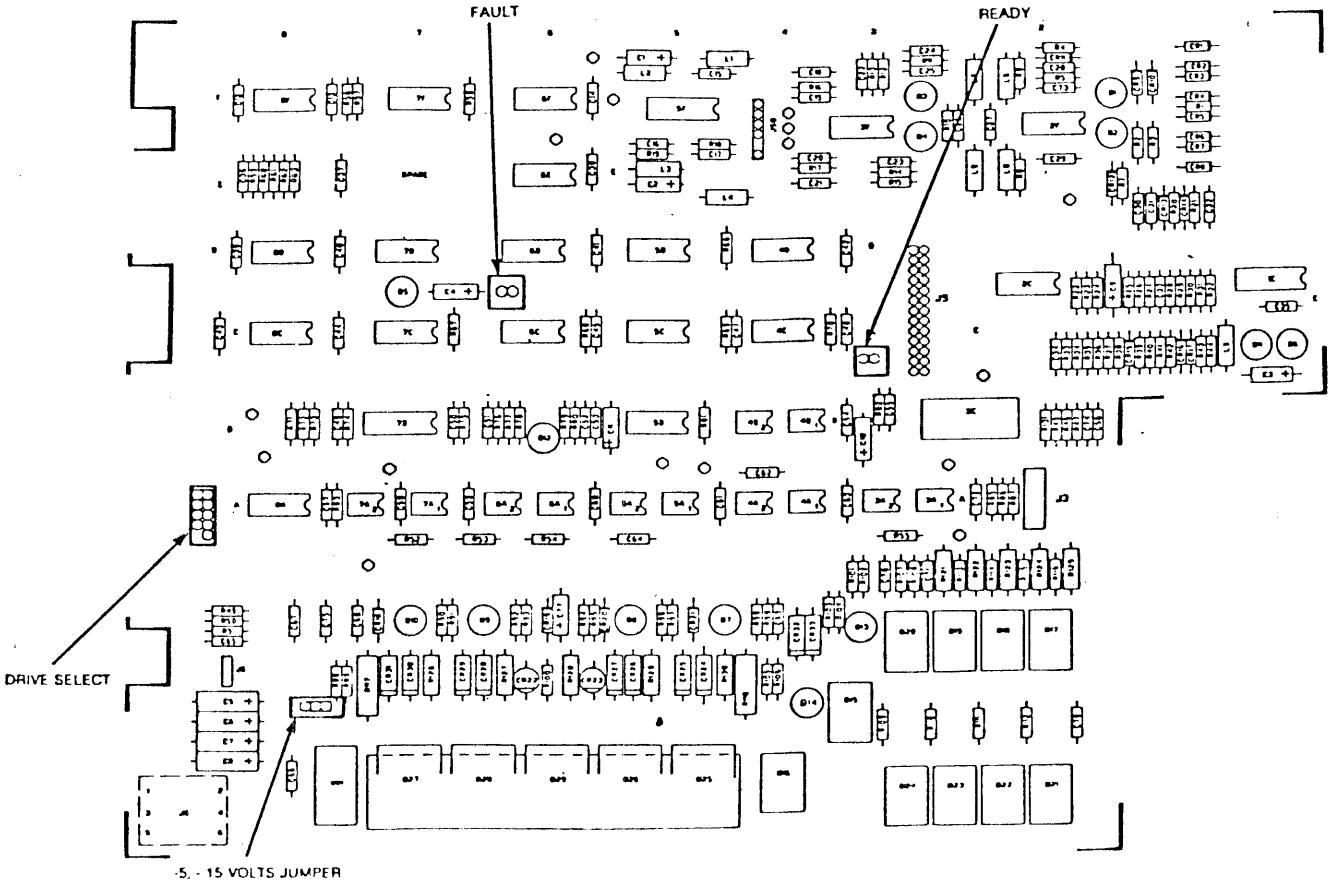


FIGURE 15. SA1000 CONTROL PCB

Section 3

Illustrated Parts Catalog

TABLE OF CONTENTS

4.0 SA1000 Illustrated Parts 30

LIST OF ILLUSTRATIONS

Figure 16. Parts Catalog 28
17. Parts Catalog 29

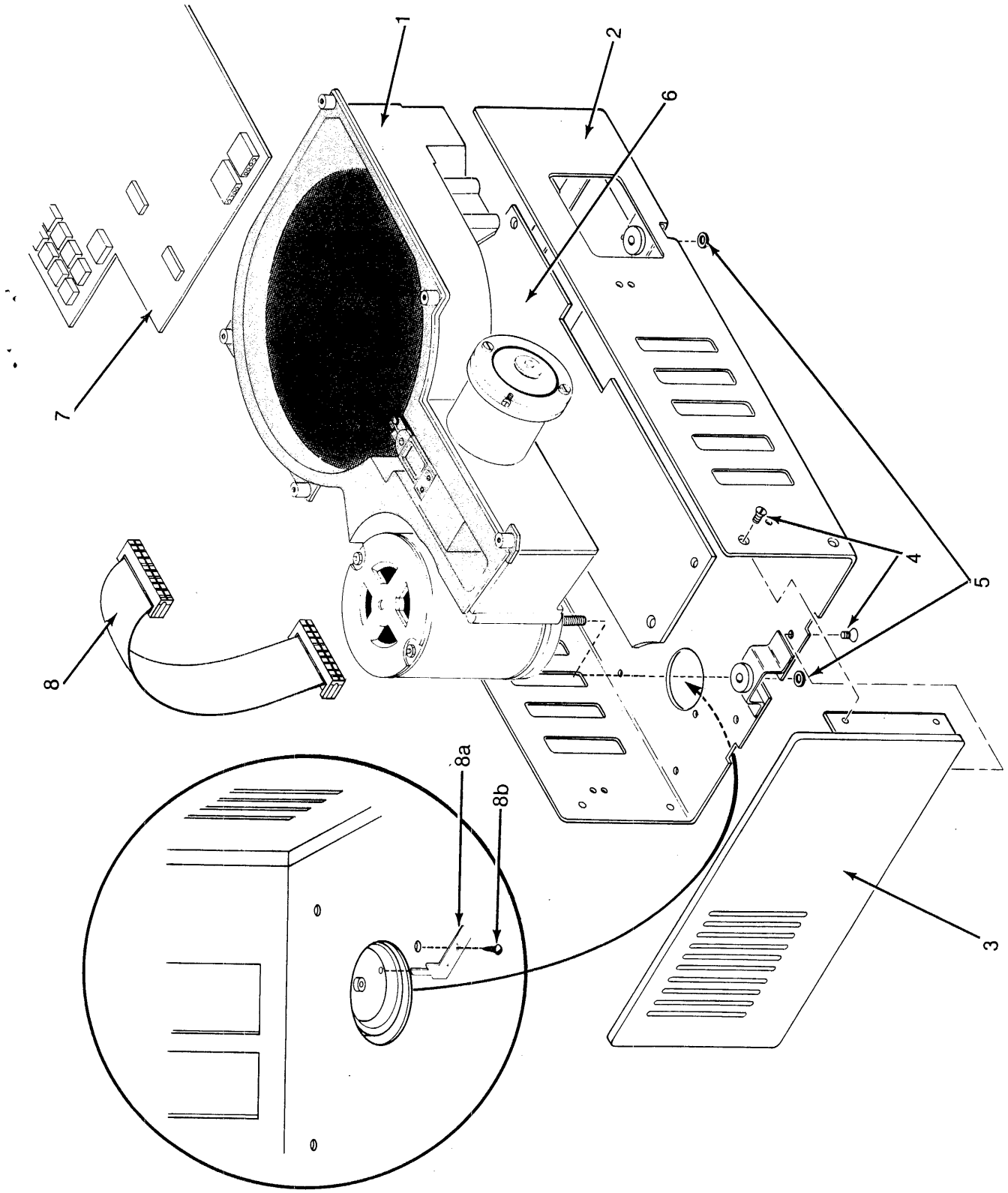


FIGURE 16. PARTS CATALOG

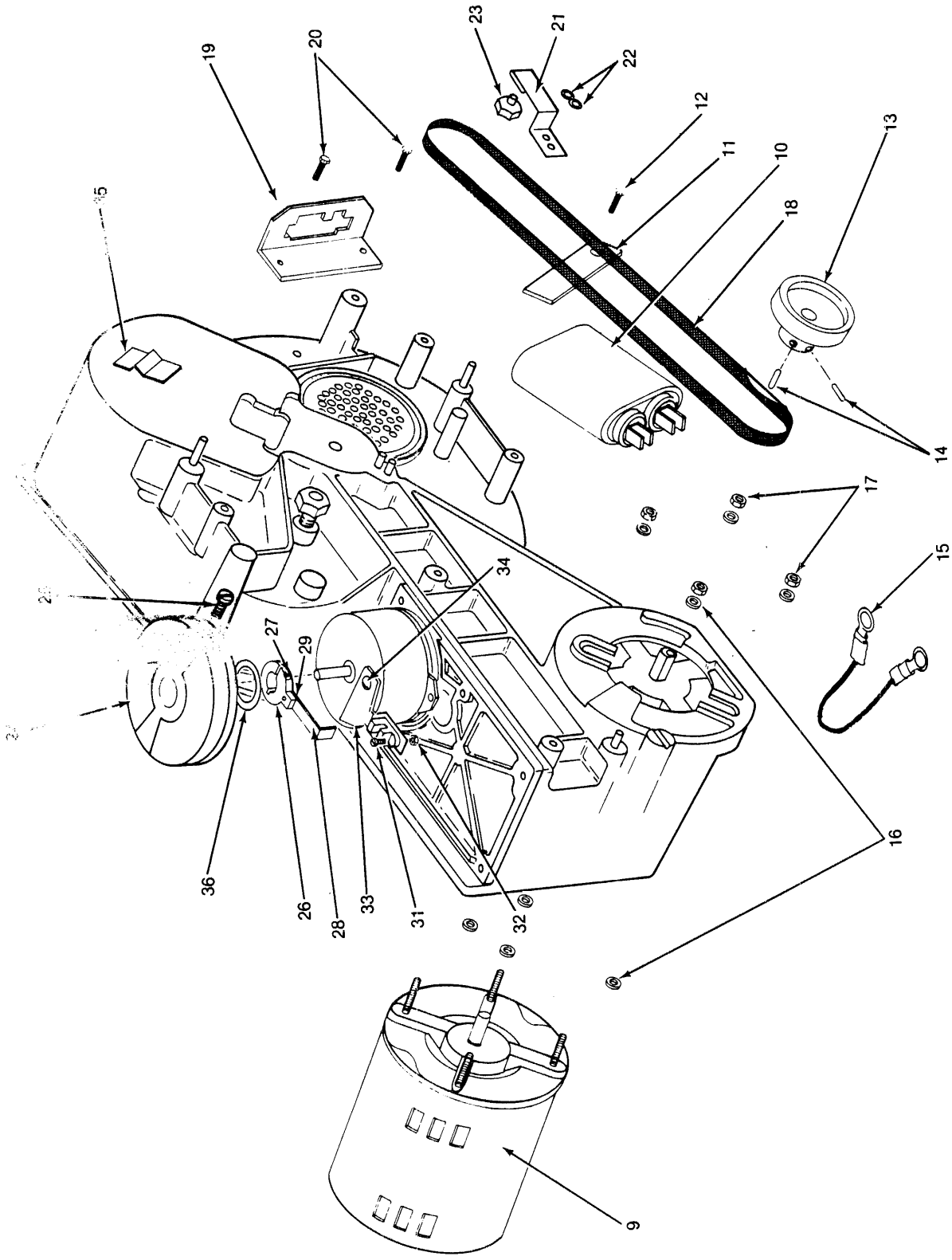


FIGURE 17. PARTS CATALOG

FIGURE 16.

REF. NO.	P/N	DESCRIPTION	QTY.
16-1	60310	Basic Drive Kit	1
—	60482	Cover Assembly, Rack	
2	60461	Rack, Bottom	1
3	60373	Rack, Front	1
4	12067	Screw	6
5	11718	Nut, Push	3
	60506	Cover Assembly, Standard	
—	60505	Cover, Bottom	1
—	60503	Cover, Front	1
—	60379	Bushing, Bottom	3
—	11719	Nut, Push	3
—	12067	Screw	6
6	26046	PCB, Stepper	1
7	26051	PCB, Control	1
8	60468	Flat Cable, PCB Interconnect	1
8a	60464	Bracket, Shipping (Spindle Lock)	1
8b	12081	Screw	1

FIGURE 17.

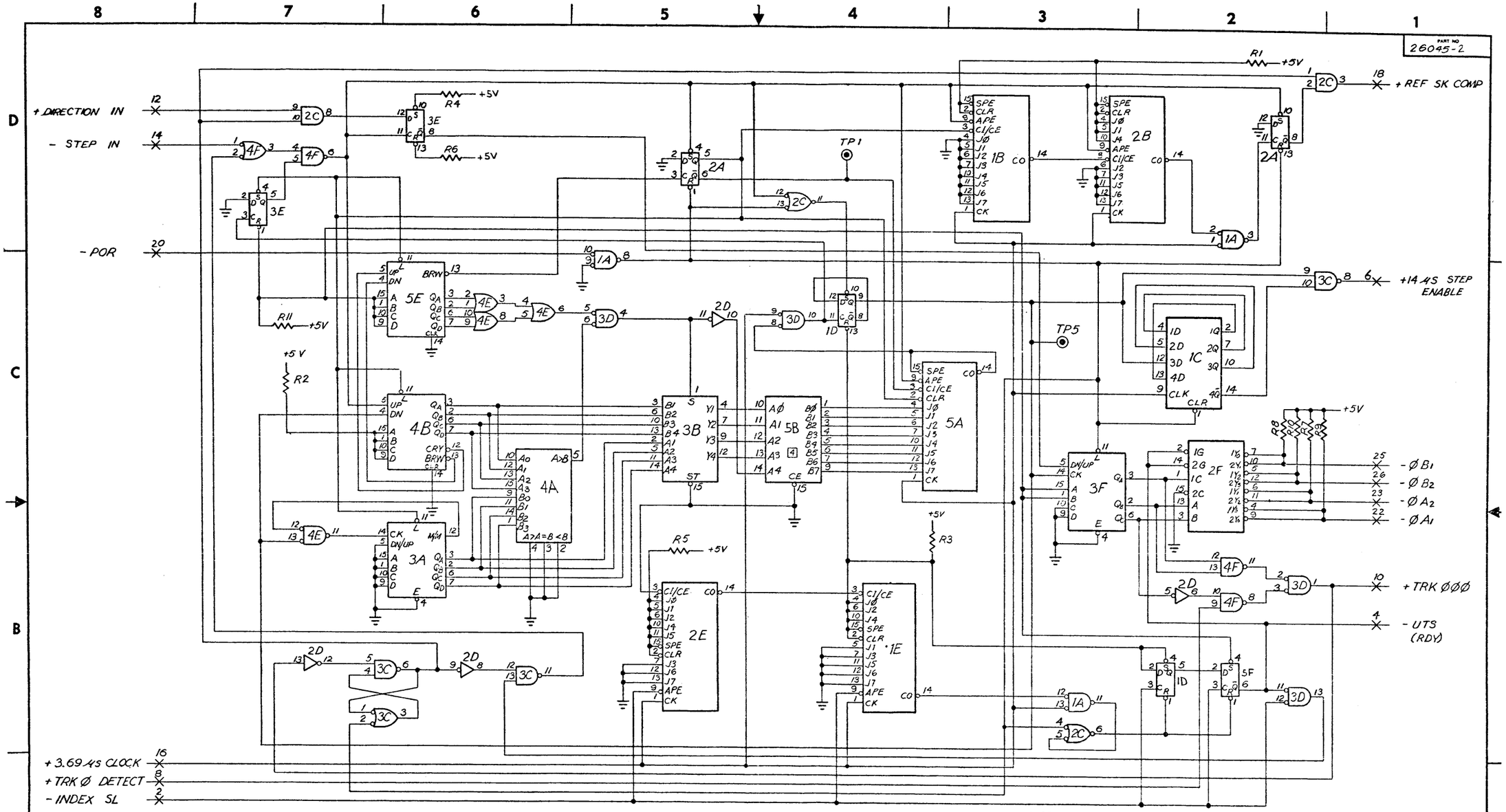
REF NO.	P/N	DESCRIPTION	QTY.
17-9	60315	110V AC Motor, Harness Asm.	1
—	60316	Motor, Spindle	1
—	15688	Receptacle, Faston	4
—	15669	Connector, Mate-N-Lok	1
—	15666	Grounding Pin	1
—	15665	Split Pin	2
10	60529	Capacitor, 5μf	1
11	60334	Bracket, Capacitor	1
12	12015	Screw	1
13	60451	Pulley, 60 Hz	1
14	12050	Set Screw	2
15	60060	AC Ground Strap	1
16	60545	Insulator, Spindle Motor	8
17	11711	Nut	4
18	60375	Belt, 60 Hz	1
19	60335	Bracket, AC Connector	1
20	12015	Screw	2
	60487	220V AC Motor, Harness Asm.	
—	60394	Motor, Spindle	1
—	15692	Receptacle, Faston	4
—	15699	Connector, AC	1
—	15666	Pin, Crimp	1
—	15665	Pin, Crimp	2
—	60529	Capacitor, 3μf	1
—	60334	Bracket, Capacitor	1
—	12015	Screw	1
—	60314	Pulley, 50 Hz	1
—	12050	Set Screw	2
—	60060	AC Ground Strap	1
—	60545	Insulator, Spindle Motor	8
—	11711	Nut	4
—	60376	Belt, 50 Hz	1
—	60335	Bracket, AC Connector	1
—		Screw	2
21	60531	Spring, Ground	1
22		Nut, Push	2
23	60533	Screw, Spindle Asm.	1
—	60532	Bolt, Spindle	1
—	60037	Pin, Spindle Ground	1
	60499	Stepper Motor Assembly	1
24	60477	Damper	1
25	60430	Screw	1
26	60417	Clamp, Track 0 Flag	1
27	11928	Screw	1
28	60404	Flag, Track 0	1
29	10170	Screw	1
30	60480	Detector, Track 0	1
31	11930	Screw	1
32	10023	Nut	1
33	60425	Mount, Track 0 Detector	1
34	10187	Screw	1
35	10440	Clip 'U'	1
36	19505	Seal, O Ring	1

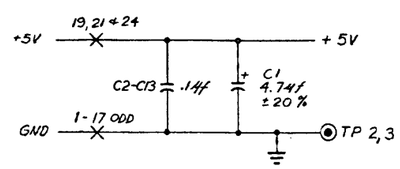
FIGURE 16.

REF. NO.	P/N	DESCRIPTION	QTY.
16-1	60310	Basic Drive Kit	1
—	60482	Cover Assembly, Rack	
2	60461	Rack, Bottom	1
3	60373	Rack, Front	1
4	12067	Screw	6
5	11718	Nut, Push	3
	60506	Cover Assembly, Standard	
—	60505	Cover, Bottom	1
—	60503	Cover, Front	1
—	60379	Bushing, Bottom	3
—	11719	Nut, Push	3
—	12067	Screw	6
6	26046	PCB, Stepper	1
7	26051	PCB, Control	1
8	60468	Flat Cable, PCB Interconnect	1
8a	60464	Bracket, Shipping (Spindle Lock)	1
8b	12081	Screw	1

FIGURE 17.

REF NO.	P/N	DESCRIPTION	QTY.
17-9	60315	110V AC Motor, Harness Asm.	1
—	60316	Motor, Spindle	1
—	15688	Receptacle, Faston	4
—	15669	Connector, Mate-N-Lok	1
—	15666	Grounding Pin	1
—	15665	Split Pin	2
10	60529	Capacitor, 5μf	1
11	60334	Bracket, Capacitor	1
12	12015	Screw	1
13	60451	Pulley, 60 Hz	1
14	12050	Set Screw	2
15	60060	AC Ground Strap	1
16	60482	Insulator, Spindle Motor	8
17	11711	Nut	4
18	60375	Belt, 60 Hz	1
19	60335	Bracket, AC Connector	1
20	12015	Screw	2
	60487	220V AC Motor, Harness Asm.	
—	60394	Motor, Spindle	1
—	15692	Receptacle, Faston	4
—	15699	Connector, AC	1
—	15666	Pin, Crimp	1
—	15665	Pin, Crimp	2
—	60529	Capacitor, 3μf	1
—	60334	Bracket, Capacitor	1
—	12015	Screw	1
—	60314	Pulley, 50 Hz	1
—	12050	Set Screw	2
—	60060	AC Ground Strap	1
—	60482	Insulator, Spindle Motor	8
—	11711	Nut	4
—	60376	Belt, 50 Hz	1
—	60335	Bracket, AC Connector	1
—		Screw	2
21	60531	Spring, Ground	1
22		Nut, Push	2
23	60533	Screw, Spindle Asm.	1
—	60532	Bolt, Spindle	1
—	60037	Pin, Spindle Ground	1
	60499	Stepper Motor Assembly	1
24	60477	Damper	1
25	60430	Screw	1
26	60417	Clamp, Track 0 Flag	1
27	11928	Screw	1
28	60404	Flag, Track 0	1
29	10170	Screw	1
30	60480	Detector, Track 0	1
31	11930	Screw	1
32	10023	Nut	1
33	60425	Mount, Track 0 Detector	1
34	10187	Screw	1
35	10440	Clip 'U'	1
36	19505	Seal, O Ring	1





REFERENCE DESIGNATION	
LAST USED	NOT USED
C13	
R11	
TP5	TP4

TYPE	POSITION	UNUSED ELEMENTS	VCC (PIN)	GRD (PIN)
7400	3C, 4F		14	7
7402	3D		14	7
7404	2D	2D, 2D2	14	7
7408	2C		14	7
7432	1A, 4E	1A2	14	7
7474	2A, 1C, 3E, 5F	5F2	16	8
7485	4A		16	8
74156	2F		16	8
74157	3B		16	8
74175	1C		16	8
74191	3A, 3F		16	8
74193	4B, 5E		16	8
CD40103B	5A, 1B, 2B, 1E, 2E		16	8
4 82S123	5B		16	8

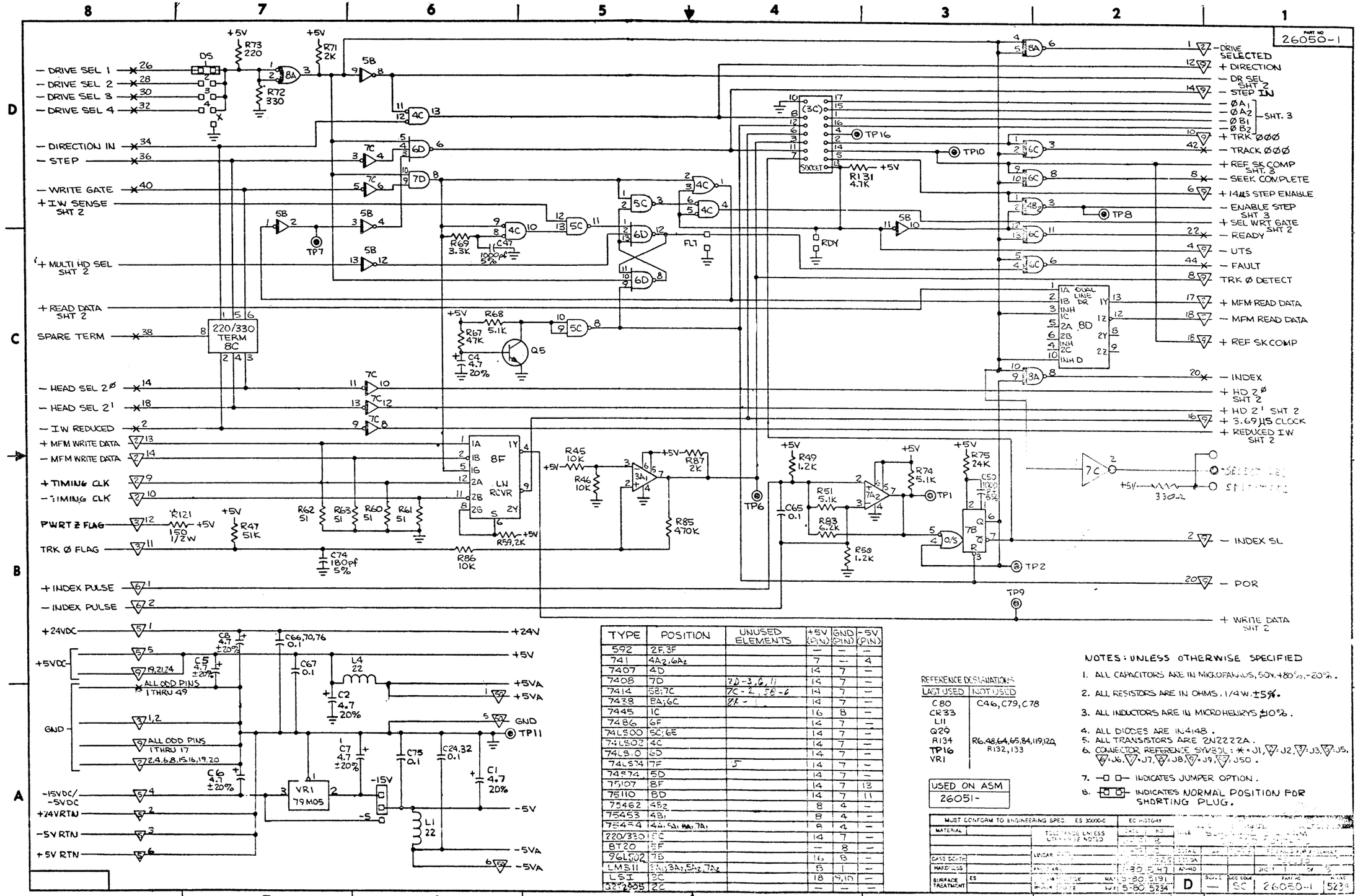
NOTES:

UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTOR VALUES ARE 2K OHMS, 1/4 W, 5%.
2. ALL CAPACITORS ARE AXIAL LEAD, 0.1 μf, 50V, +80-20%
3. 74 LS SERIES IC'S MAY BE USED.

4 I.C., PROM, RAMP CNTL.

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0		EC HISTORY		SHUGART ASSOCIATES
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	DATE	NO.	TITLE [illegible] DIAGRAM STEPPER LOGIC
CASE DEPTH	LINEAR ±.XX ±.XXX	[illegible]	52M	DETAIL [illegible] 12/7[illegible] RELEASED FOR ASSEMBLY 26045
HARDNESS	ANGULAR±			APPRO [illegible] SHEET 1 OF 1
SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX INSIDE MAX			D SCALE — DOC CODE SC PART NO. 26045-2 REV EC 52A



TYPE	POSITION	UNUSED ELEMENTS	+5V (PIN)	GND (PIN)	-5V (PIN)
592	2F, 3F		—	—	—
741	4A2, 6A2		7	—	4
7407	4D		14	7	—
7408	7D	2D-3, 6, 11	14	7	—
7414	5B; 7C	7C-2, 5B-6	14	7	—
7438	8A; 6C	8A -	14	7	—
7445	1C		16	8	—
7486	6F		14	7	—
74LS00	5C; 6E		14	7	—
74LS02	4C		14	7	—
74LS10	6D		14	7	—
74LS74	7F	5	14	7	—
74S74	5D		14	7	—
75107	8F		14	7	13
75110	8D		14	7	11
75462	4B2		8	4	—
75453	4B1		8	4	—
75454	4A1, 5A1, 6A1, 7A1		8	4	—
220/330	8C		14	7	—
8T20	8F		—	8	—
96LS02	7B		16	8	—
LM311	3A1, 3A2, 5A2, 7A2		8	1	—
LSI	2C		18	9,10	—
3875-005	2C		—	—	—

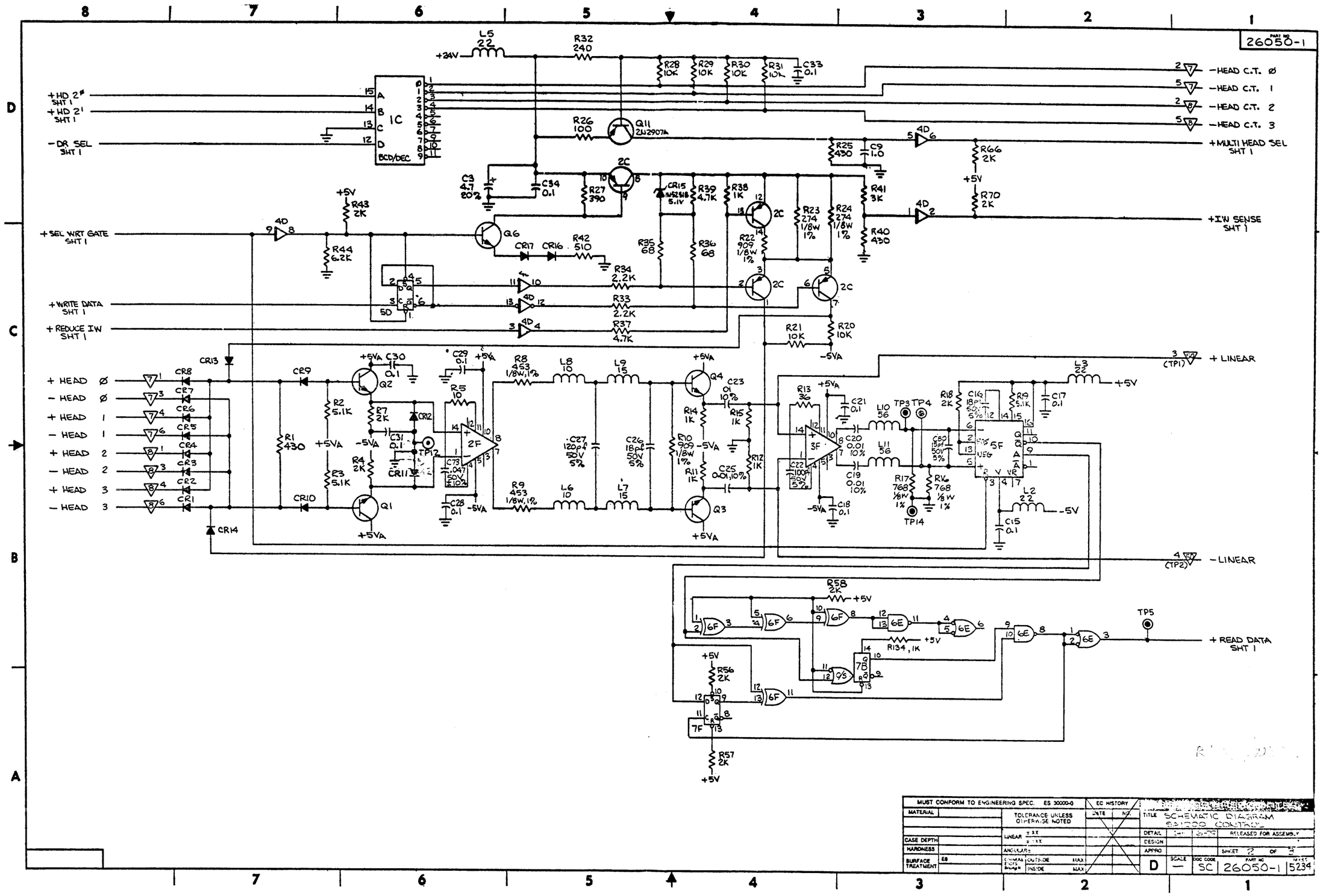
REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C80	C46, C79, C78
CR33	
L11	
Q29	
R134	R6, 48, 64, 65, 84, 119, 120, R132, 133
TP16	
VR1	

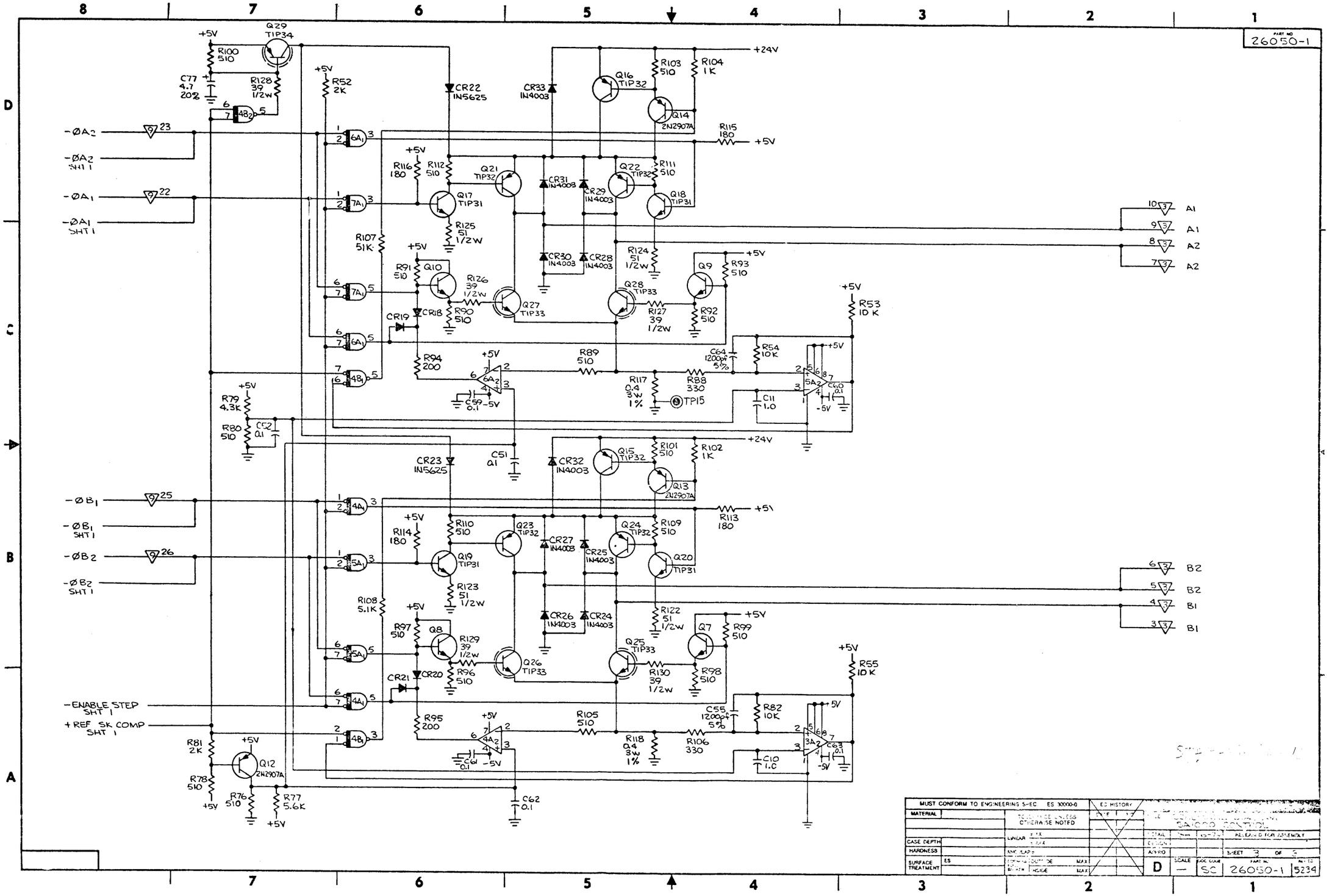
USED ON ASM
26051-

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITORS ARE IN MICROFARADS, 50V, +80%, -20%.
2. ALL RESISTORS ARE IN OHMS, 1/4W, ±5%.
3. ALL INDUCTORS ARE IN MICROHENRYS ±10%.
4. ALL DIODES ARE IN4148.
5. ALL TRANSISTORS ARE 2N2222A.
6. CONNECTOR REFERENCE SYMBOL: ✳=J1, ▽=J2, ▽=J3, ▽=J5, ▽=J6, ▽=J7, ▽=J8, ▽=J9, ▽=J50.
7. —o o— INDICATES JUMPER OPTION.
8. INDICATES NORMAL POSITION FOR SHORTING PLUG.

MUST CONFORM TO ENGINEERING SPEC ES 30000-C
EC HISTORY
MATERIAL
TOLERANCE UNLESS OTHERWISE NOTED
CASE DEPTH
HARDNESS
SURFACE TREATMENT ES
MAY 19-80 5191
JUNE 5-80 5234
D
SIZE — ACC CODE SC PART NO 26050-1 REV 523


26050-1
+HD 2Ø SHT 1
+HD 2¹ SHT 1
-DR SEL SHT 1
+SEL WRT GATE SHT 1
+WRITE DATA SHT 1
+REDUCE IW SHT 1
+HEAD Ø
-HEAD Ø
+HEAD 1
-HEAD 1
+HEAD 2
-HEAD 2
+HEAD 3
-HEAD 3
-HEAD C.T. Ø
-HEAD C.T. 1
-HEAD C.T. 2
-HEAD C.T. 3
+MULTI HEAD SEL SHT 1
+IW SENSE SHT 1
+LINEAR
-LINEAR
+READ DATA SHT 1
MUST CONFORM TO ENGINEERING SPEC. ES 30000-0
EC HISTORY
TOLERANCE UNLESS OTHERWISE NOTED
TITLE SCHEMATIC DIAGRAM
RELEASED FOR ASSEMBLY
SHEET 2 OF 3
D
SC
26050-1
5234



26050-1
-ØA2
-ØA2 SHT 1
-ØA1
-ØA1 SHT 1
-ØB1
-ØB1 SHT 1
-ØB2
-ØB2 SHT 1
-ENABLE STEP SHT 1
+REF SK COMP SHT 1
A1
A2
B2
B1
+24V
+5V
-5V
TP15
MUST CONFORM TO ENGINEERING SPEC ES 30000-0
MATERIAL
CASE DEPTH
HARDNESS
SURFACE TREATMENT
TOLERANCE UNLESS OTHERWISE NOTED
EC HISTORY
SA1000 CONTROL
RELEASED FOR ASSEMBLY
SHEET 3 OF 3
D
SCALE
SC
26050-1
5234

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